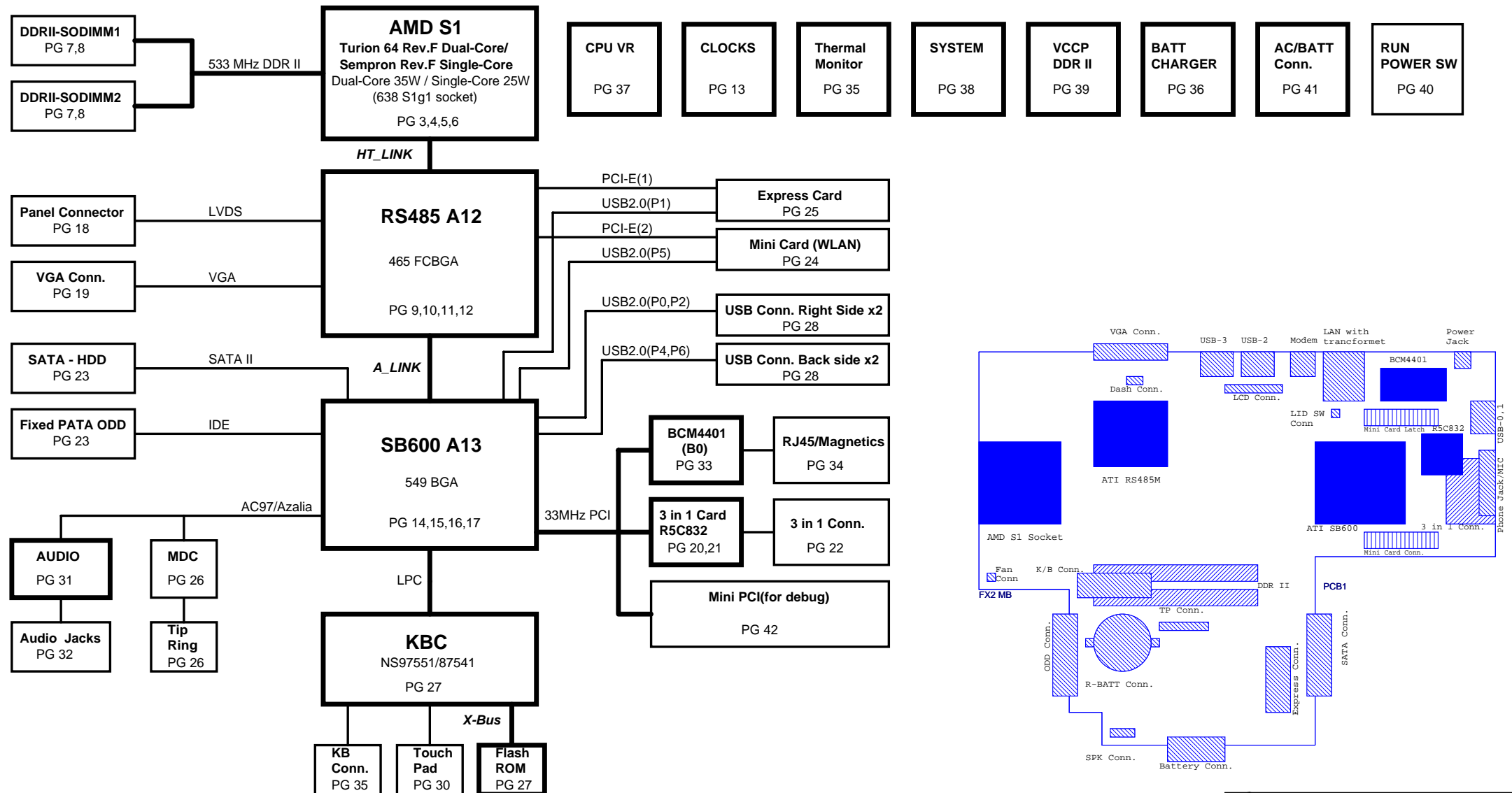


Kirin (FX2 with NS)

VER : 1A

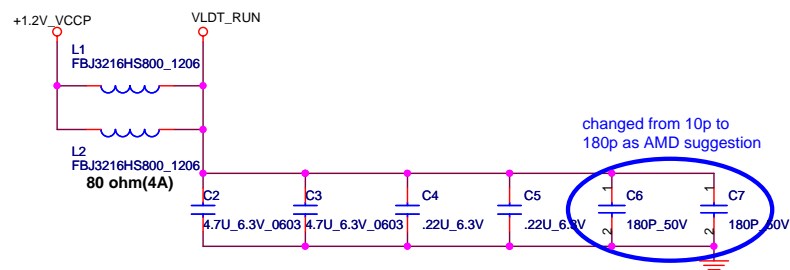
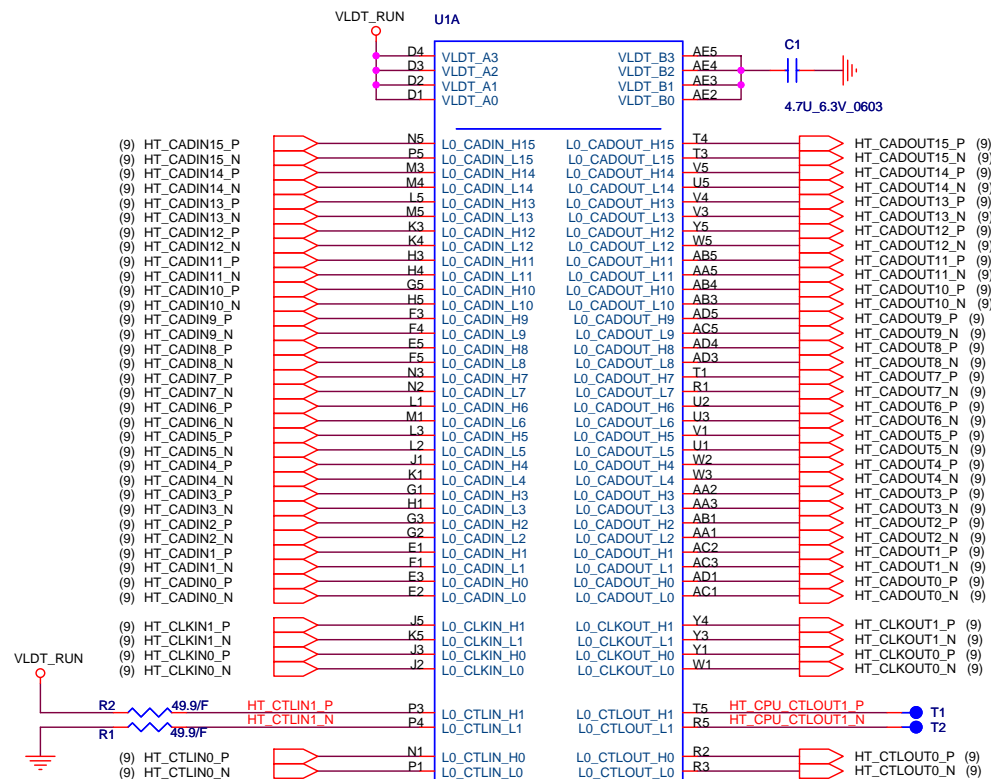


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1	BLOCK DIAGRAM
2	FRONT PAGE
3	ATHLON64 HT I/F
4	ATHLON64 DDRII MEMORY
5	ATHLON64 CTRL & DEBUG
6	ATHLON64 PWR & GND
7	DDRII SODIMMX2
8	DDRII TERMINATION
9	RS485-HT LINK0 I/F
10	RS485-PCIE LINK I/F
11	RS485-LVDS
12	RS485-POWER
13	CLOCK GENERATOR
14	SB600M-PCIE/PCI/LPC
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16	SB600M HDD/POWER
17	SB600M STRAPS
18	LCD CONN
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20	5C832/PCI
21	CARD READER
22	CARD READER CONN
23	SATA HDD & PATA ODD
24	MINI Card
25	MINI Card
26	MDC CONN
27	PC97551 & FLASH
28	USB
29	EMI & Screw hole
30	SWITCH & TP & LED
31	Azelia CODEC
32	AUDIO CONN
33	LAN(BCM4401)
34	LAN JACK
35	KB & THERMAL & FAN
36	CHARGER (MAX8731)
37	VHCORE (MAX8774)
38	SYSTEM (MAX8734)
39	VCCP & DDR2 (MAX8743)
40	RUN POWER SW
41	DCIN,Batt
42	MINI PCI(for debug)
43	Power On Sequence
44	Power On Diagram
45	SMBUS BLOCK

**PROCESSOR HYPERTRANSPORT INTERFACE**

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

**LAYOUT: Place bypass cap on topside of board**

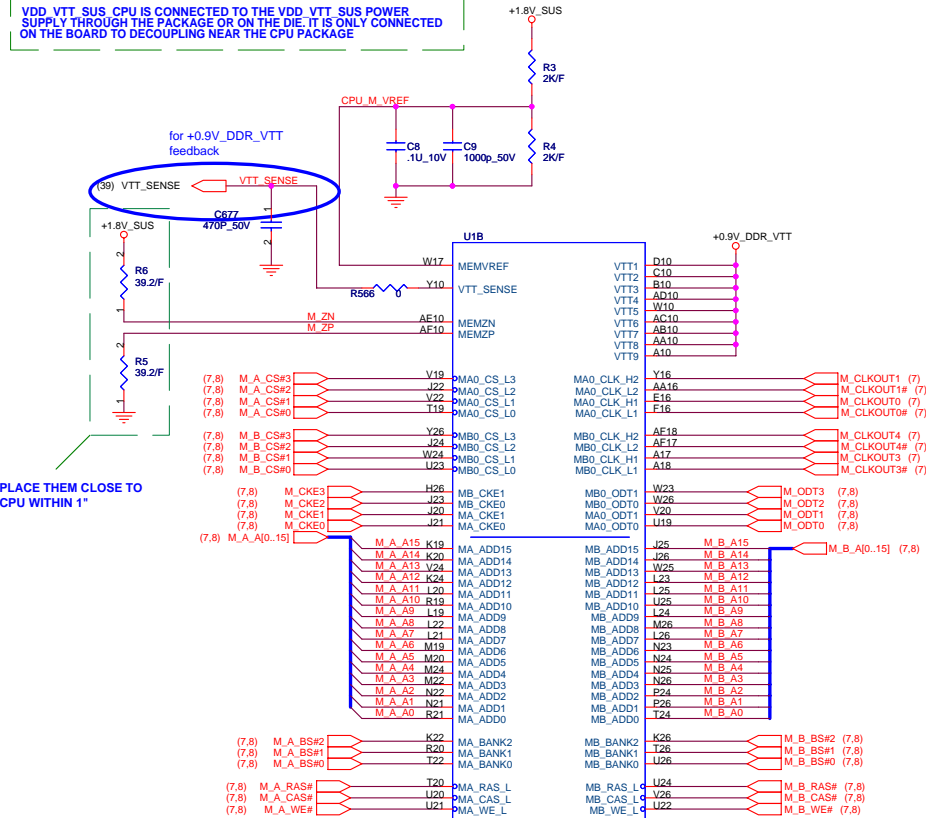
NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS



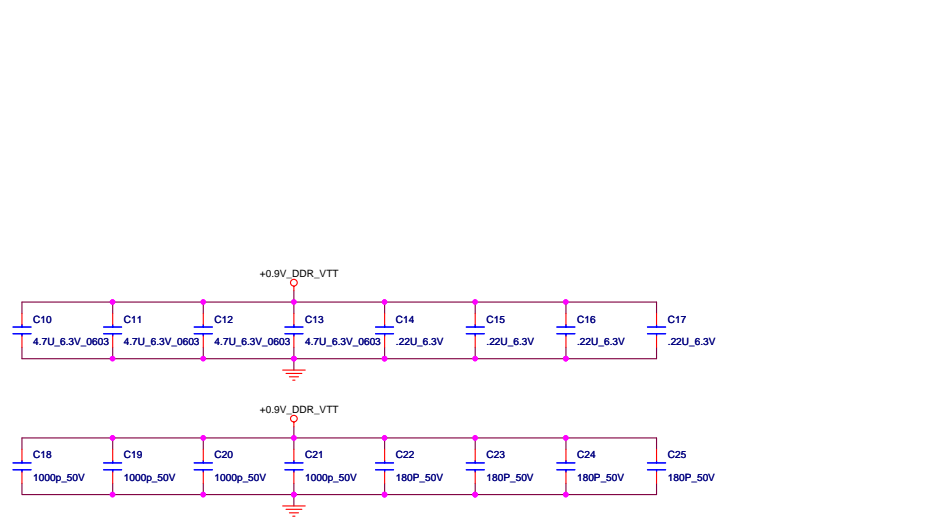
**QUANTA
COMPUTER**

Title		
ATHLON64 HT I/F		
Size	Document Number	Rev
	FX2	1A
Date:	Friday, May 05, 2006	Sheet 3 of 47

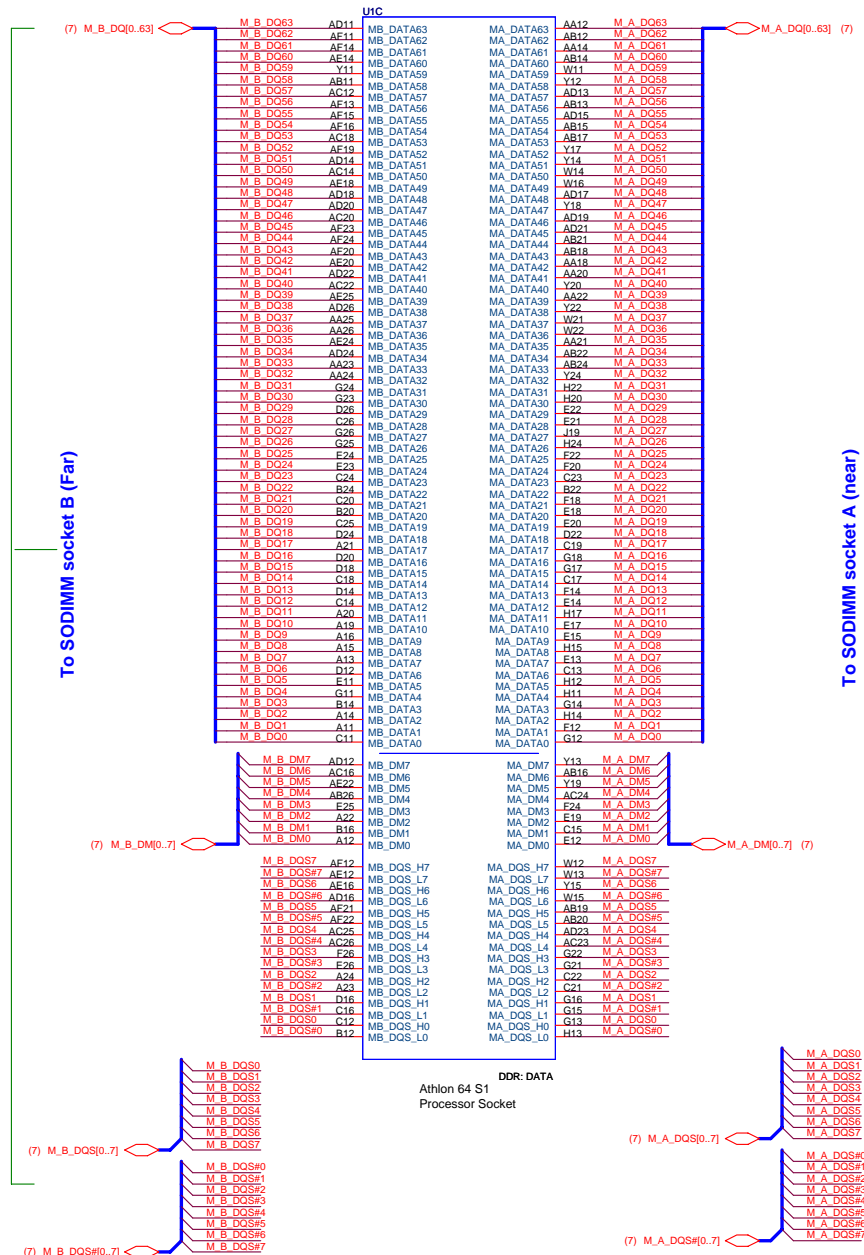
VDD_VTT_SUS CPU IS CONNECTED TO THE VDD_VTT_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



DDR II: CMD/CTRL/CLK
Athlon 64 S1
Processor Socket

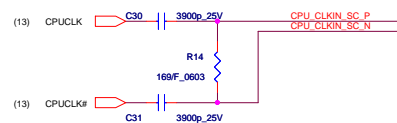


Processor DDR2 Memory Interface

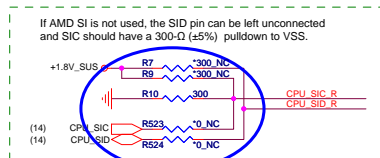


DDR: DATA
Athlon 64 S1
Processor Socket

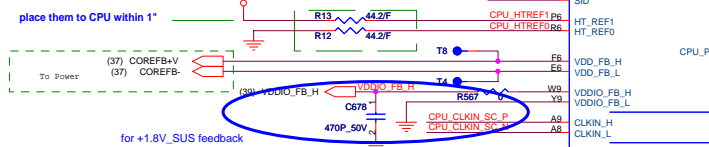




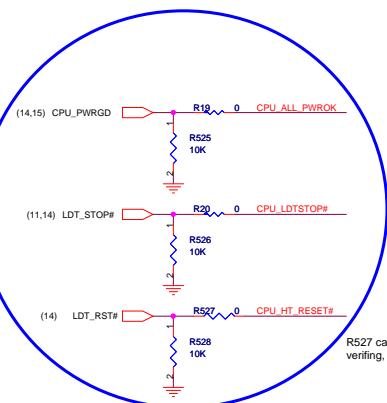
R14 close U1 within 600 mil , C30
& C31 close U1 within 1250 mil



for CPU rev.F , if for rev.G , populate R7,R9,R523,R524 and depopulate R10

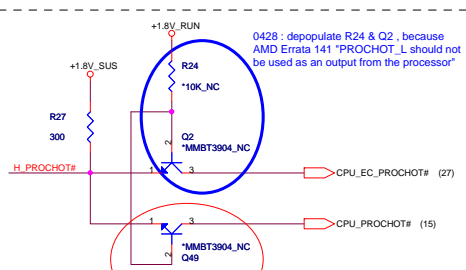


for +1.8V_SUS feedback



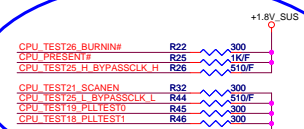
change for SB600 from SB460

R527 can be used for EMI
verifying, place close to CPU



SB this pin is 3.3V, need it level-shift.

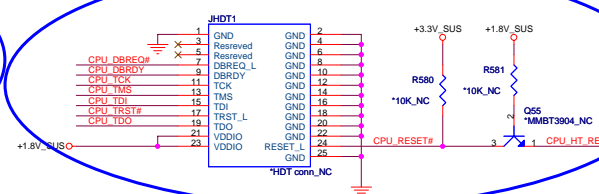
```
delete ED5 H_THERMTRIP# circuit
```



If no use which Net
need pull-up or down

change TEST 12/14/15/20/22/24/27 to be NC pin without pull up or pull down

add HDT connector for debug convenience



HDT CONNECTOR



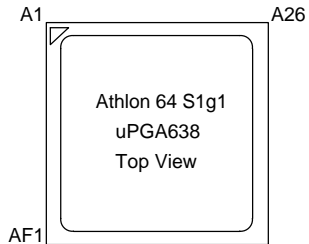
**QUANTA
COMPUTER**

ATHLON64 CTRL & DEBUG

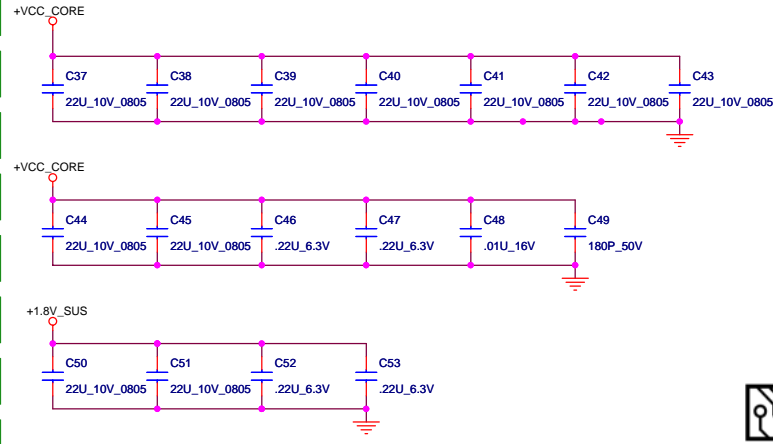
Size	Document Number FX2
------	------------------------

Date: Friday, May 05, 2006

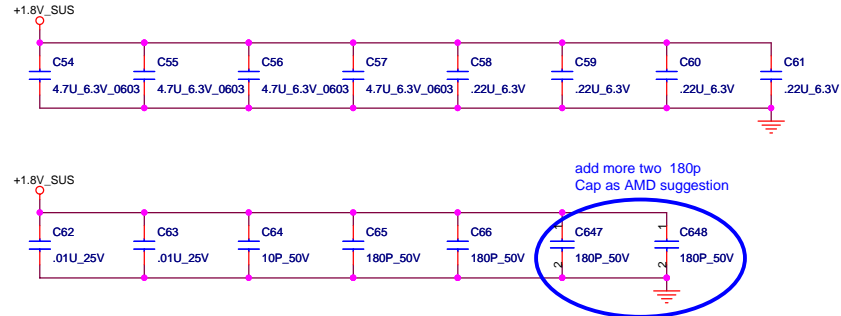
Rev
1A



BOTTOMSIDE DECOUPLING

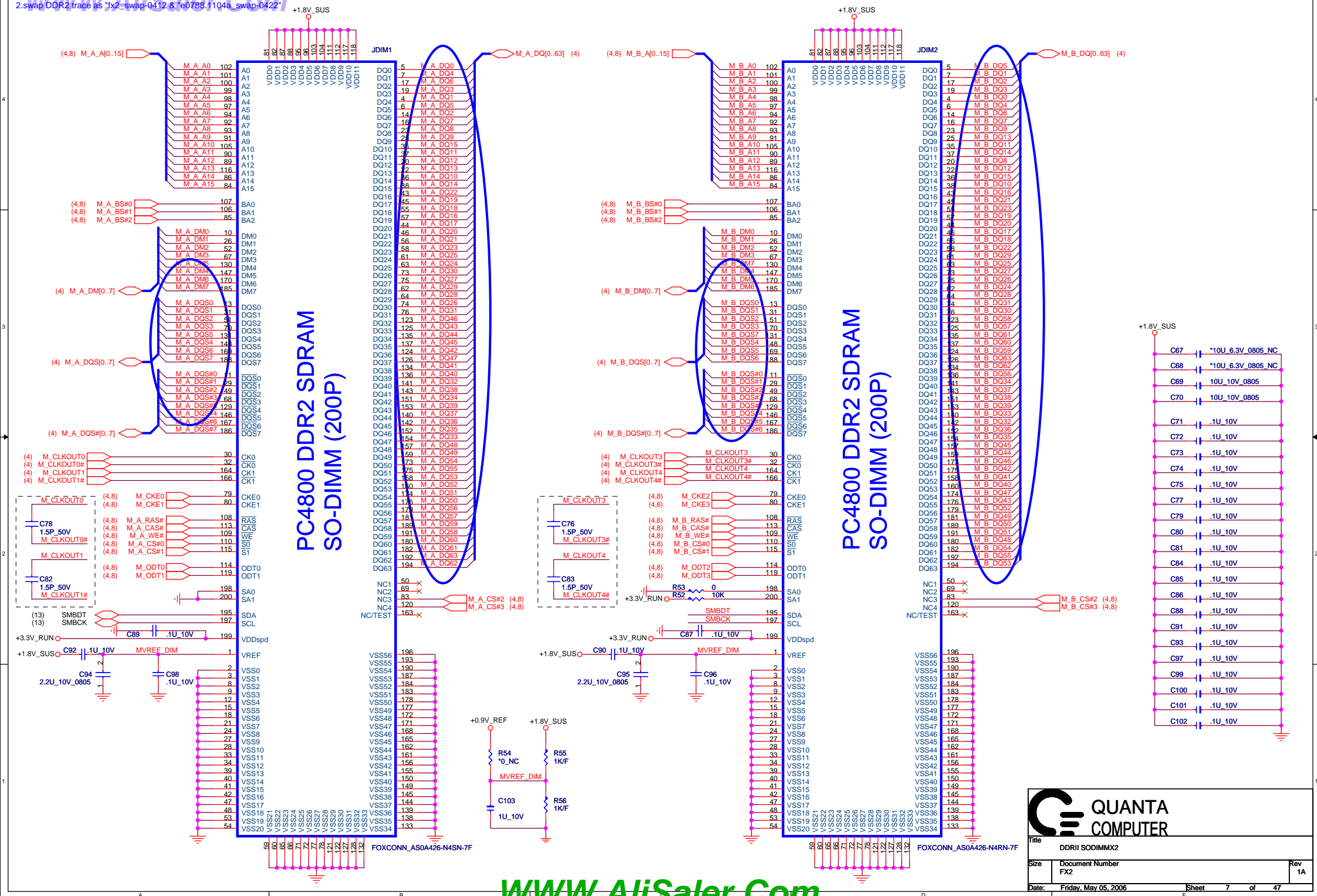


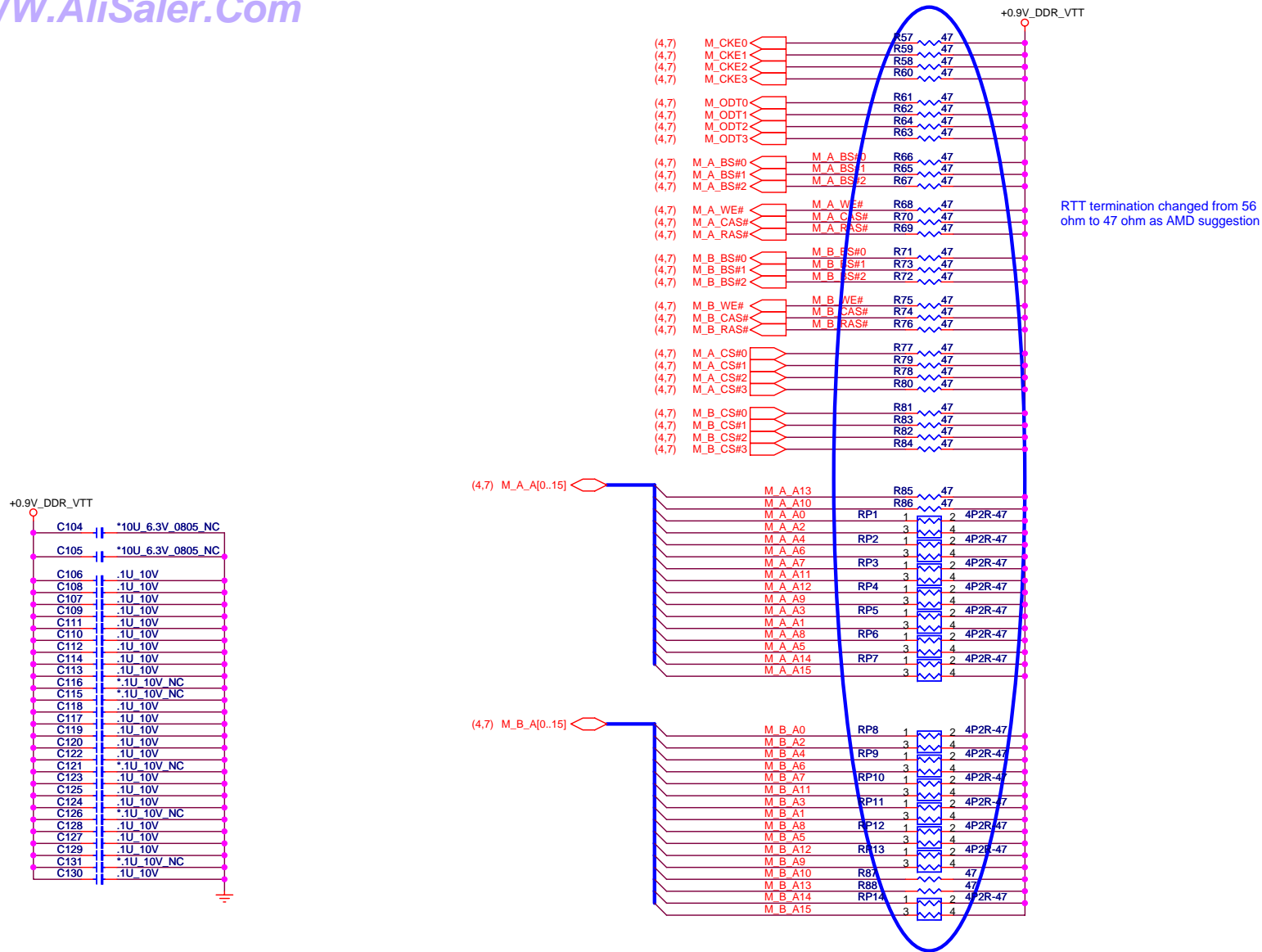
DECOUPLING BETWEEN PROCESSOR AND DIMMs PLACE CLOSE TO PROCESSOR AS POSSIBLE




PROCESSOR POWER AND GROUND

- 1.Change DDR2 socket(P/N, Description, footprint, part reference, value)
- 2.swap DDR2 trace as "fx2_swap-0412 & "e0788.1104a_swap-0422"

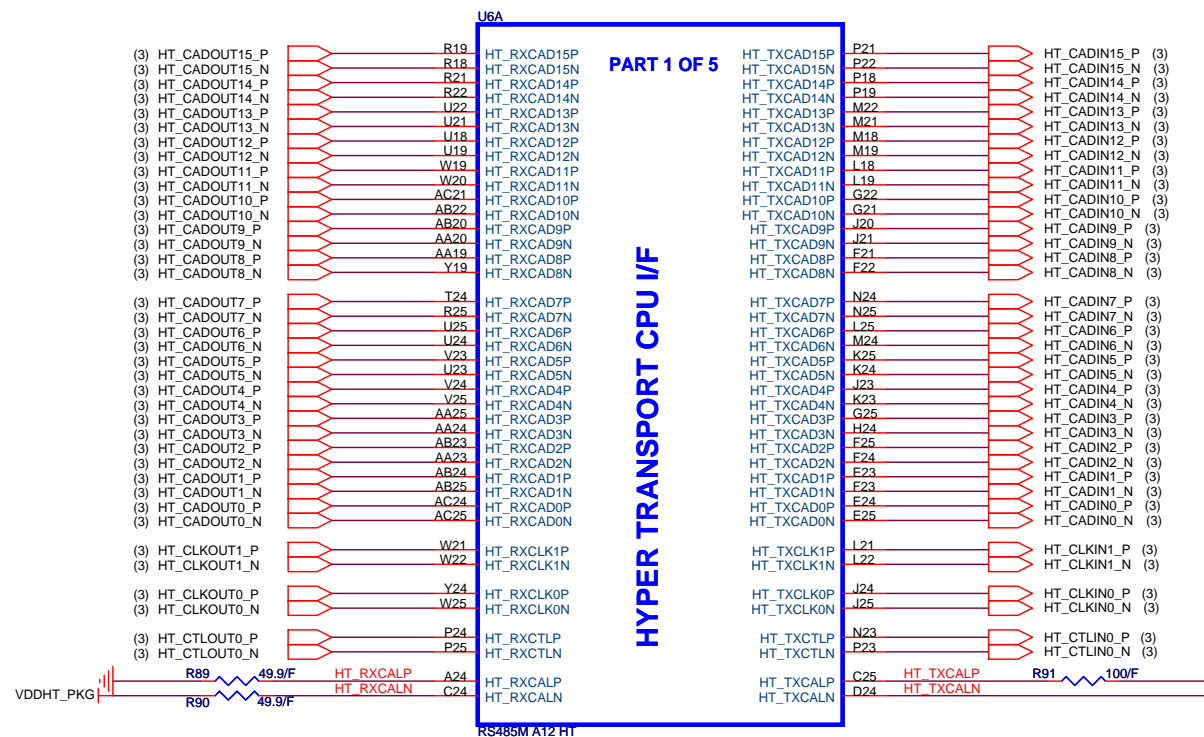






QUANTA
COMPUTER

Title DDR2 TERMINATION		
Size	Document Number FX2	Rev 1A
Date	Friday, May 05, 2006	Sheet 8 of 47

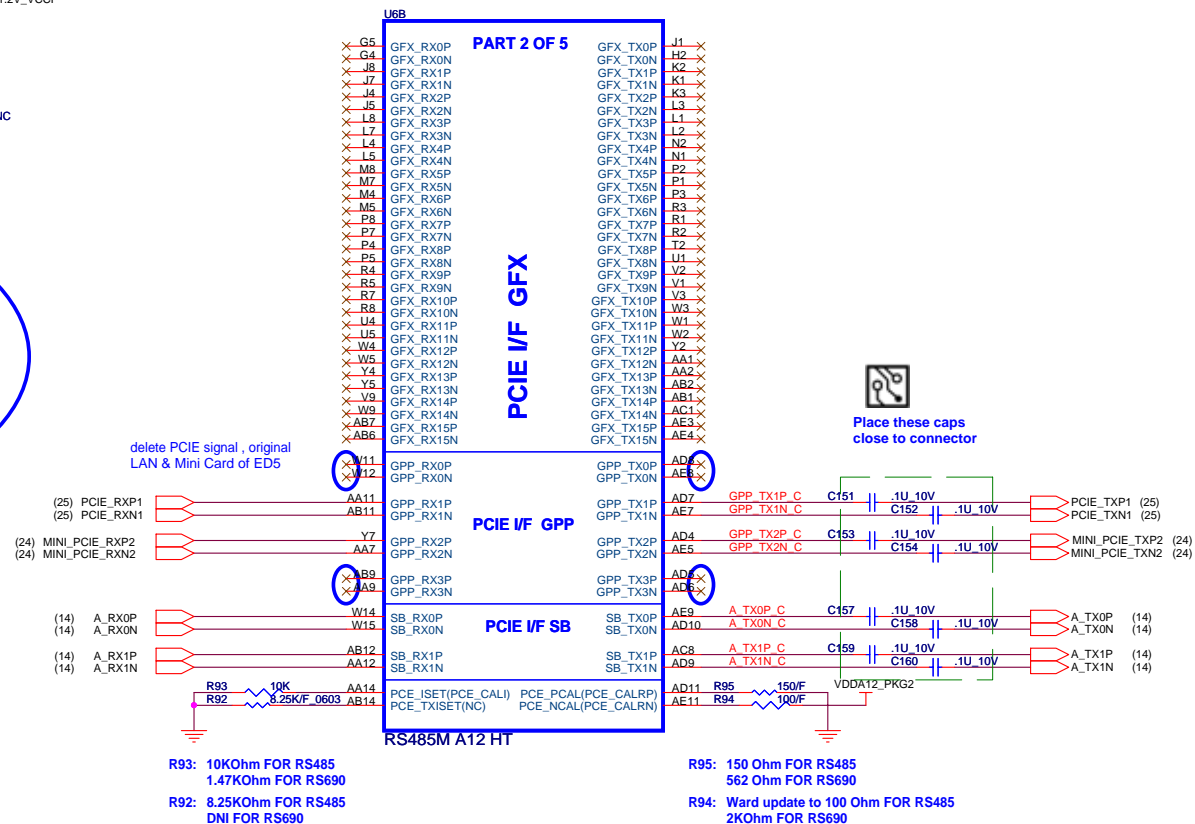


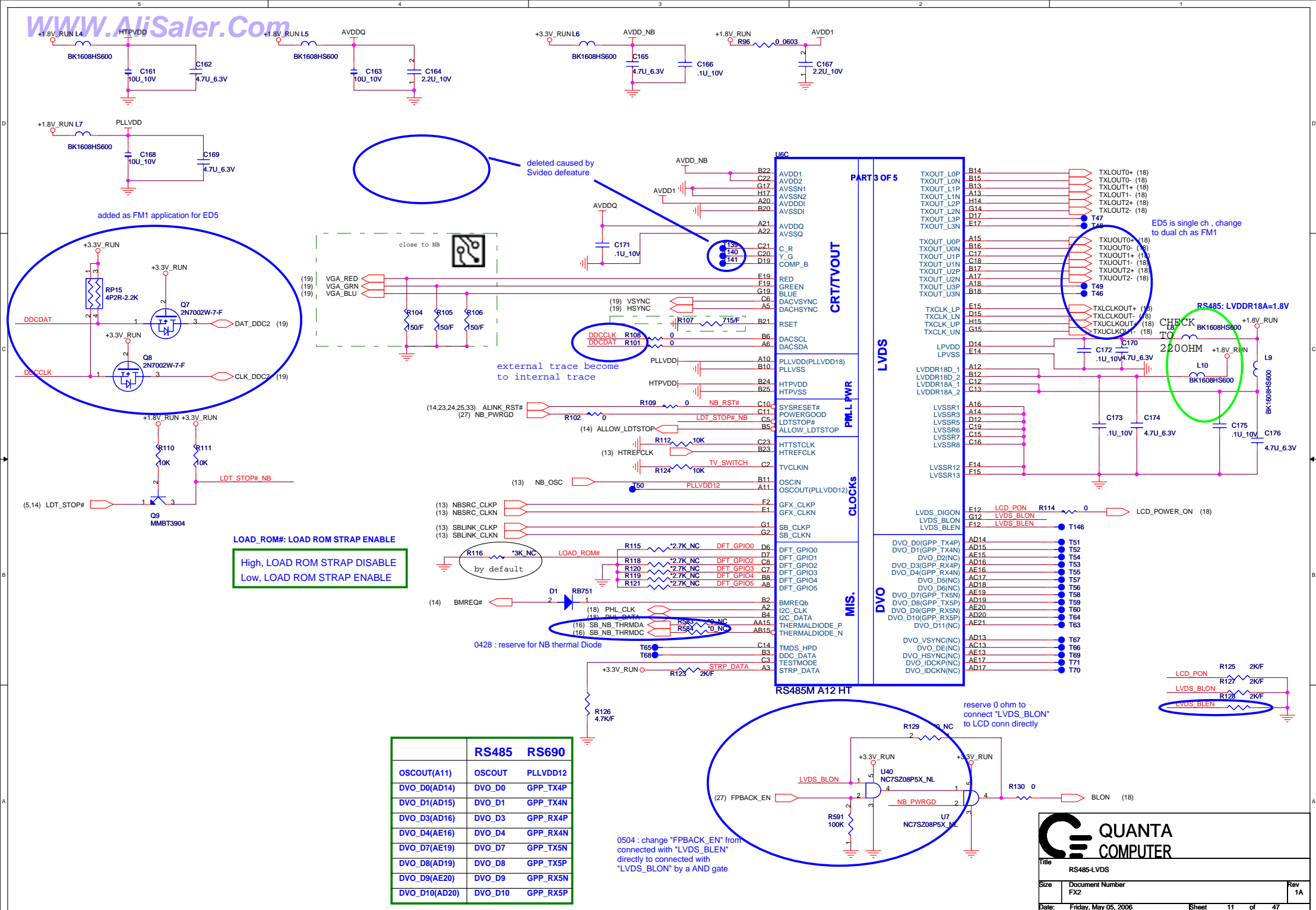
QUANTA
COMPUTER

Title RS485-HT LINK0 I/F

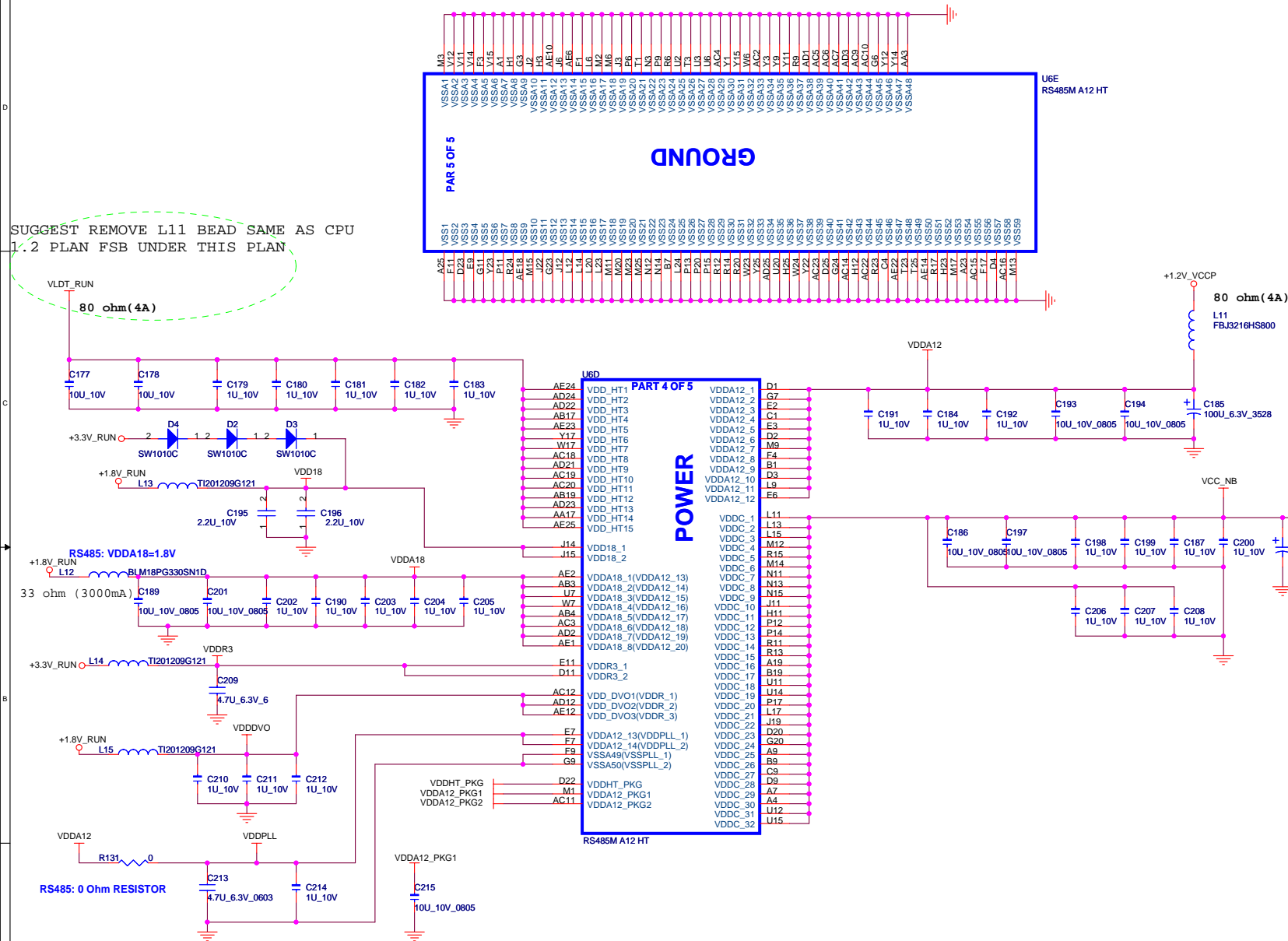
Size Document Number FX2 Rev 1A

Date: Friday, May 05, 2006 Sheet 9 of 47





SUGGEST REMOVE L11 BEAD SAME AS CPU
1.2 PLAN FSB UNDER THIS PLAN



NB RS485 POWER STATES

Power Signal	S0	S1	S3	S4/S5	G3
VDDHT	ON	ON	OFF	OFF	OFF
VDDR	ON	ON	OFF	OFF	OFF
VDD18	ON	ON	OFF	OFF	OFF
VDVC	ON	ON	OFF	OFF	OFF
VDDA18	ON	ON	OFF	OFF	OFF
VDDA12	ON	ON	OFF	OFF	OFF
AVDD	ON	ON	OFF	OFF	OFF
AVDDDI	ON	ON	OFF	OFF	OFF
PLLVD	ON	ON	OFF	OFF	OFF
HTPVDD	ON	ON	OFF	OFF	OFF
VDDR3	ON	ON	OFF	OFF	OFF
LPVDD	ON	ON	OFF	OFF	OFF
LVDDR18D	ON	ON	OFF	OFF	OFF
LVDDR18A	ON	ON	OFF	OFF	OFF

QUANTA
COMPUTER

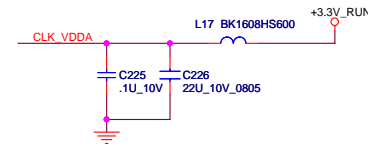
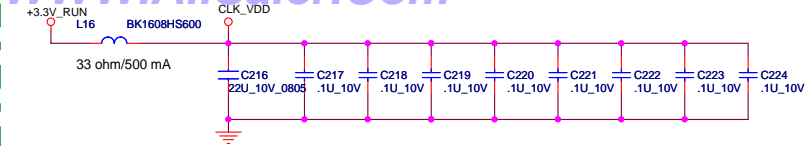
Title: RS485-POWER

Size: Document Number FX2

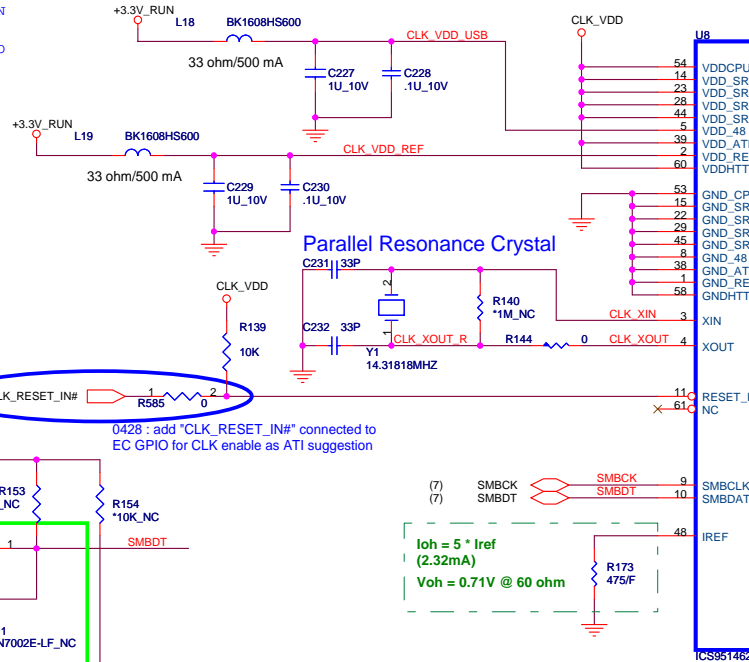
Date: Thursday, May 04, 2006

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Rev: 1A



- 1- PLACE ALL SERIAL TERMINATION RESISTORS CLOSE TO U800
- 2- PUT DECOUPLING CAPS CLOSE TO Clock Gen. POWER PIN



(27) CLK_RESET_IN#

042B: add "CLK_RESET_IN#" connected to EC GPIO for CLK enable as ATI suggestion

become to no used as FM1 application

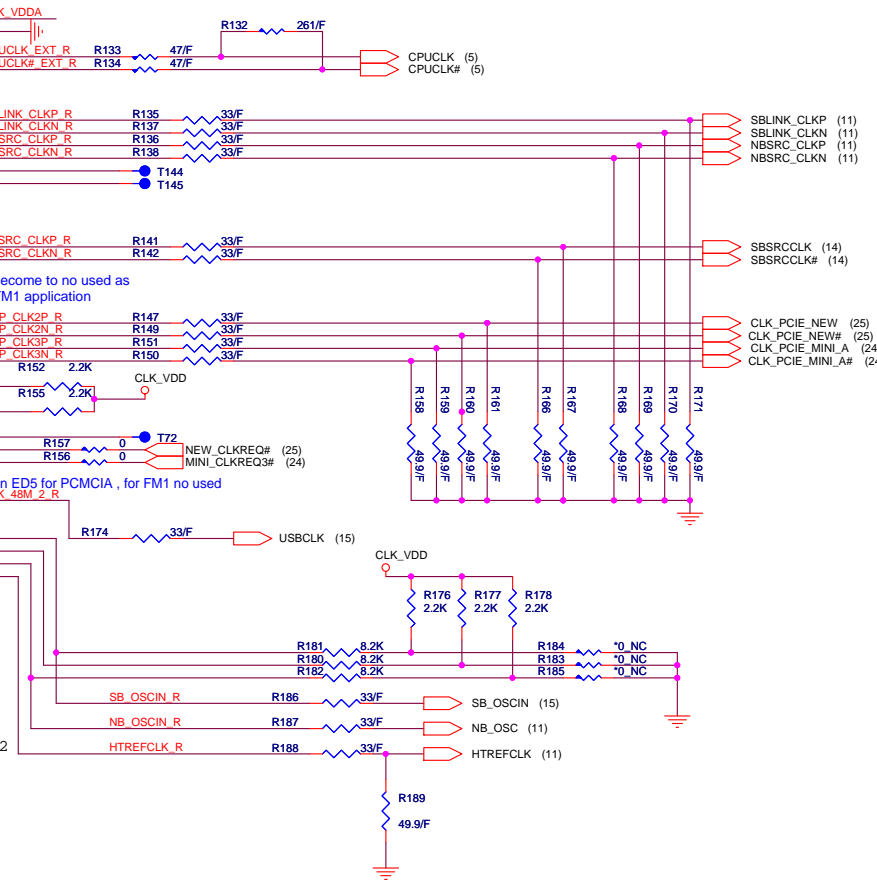
on ED5 for PCMCIA, for FM1 no used

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

Check AMD clock

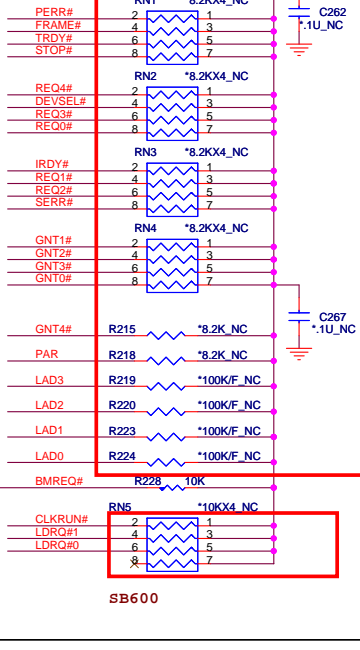
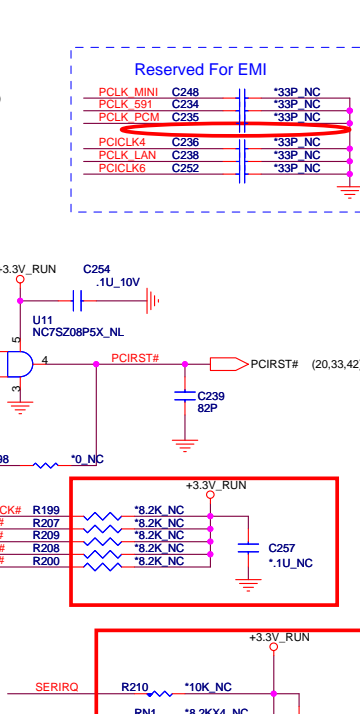
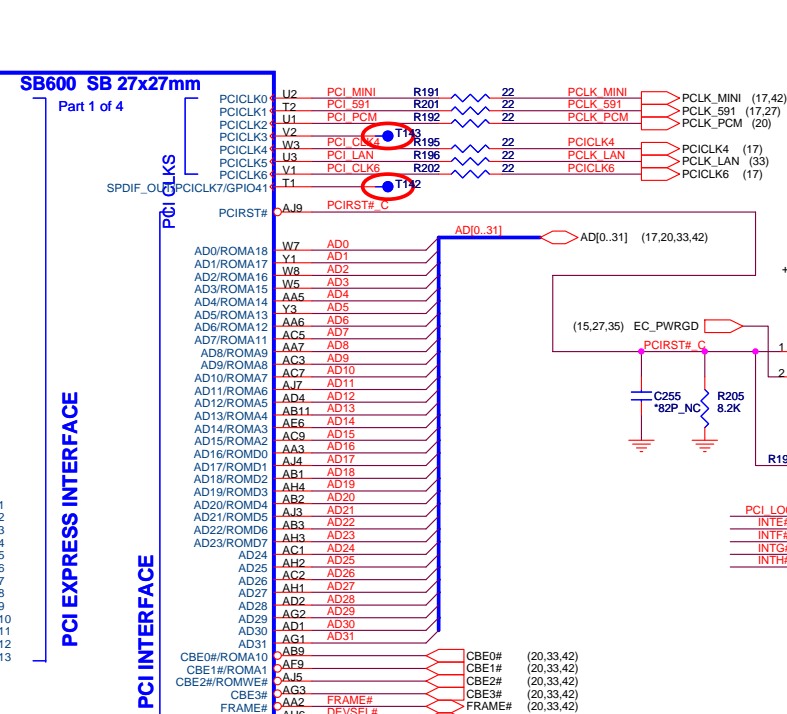
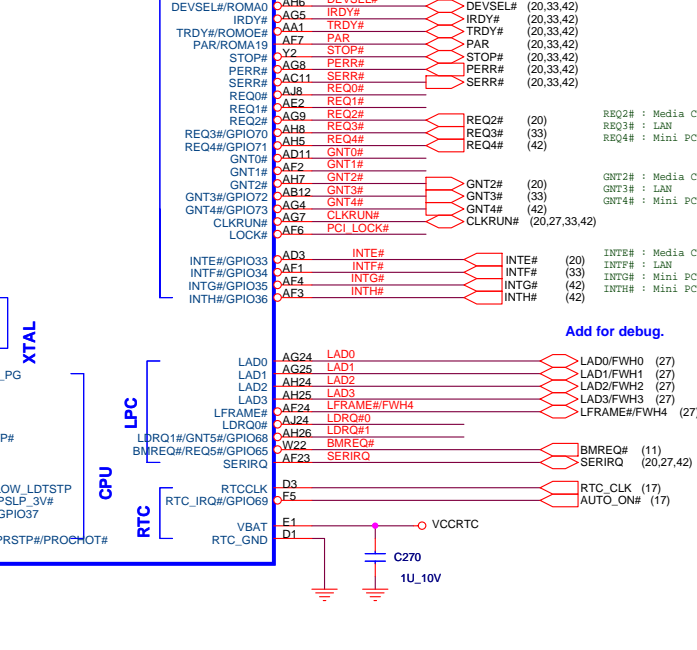
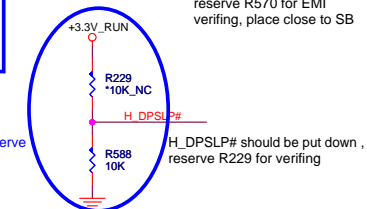
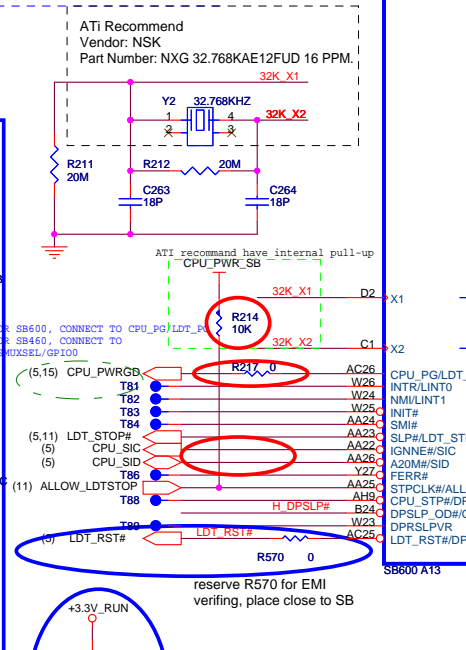
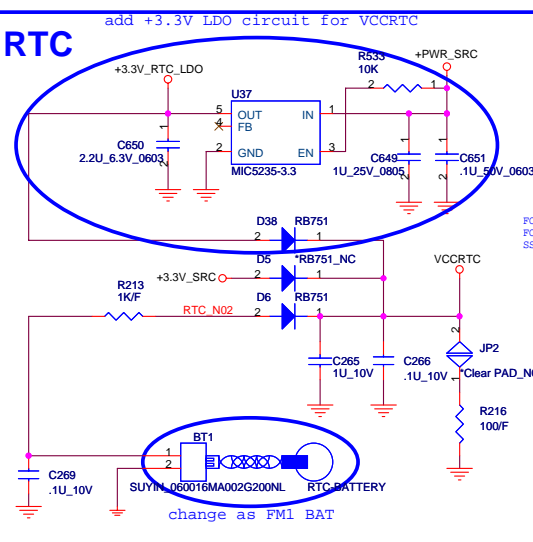
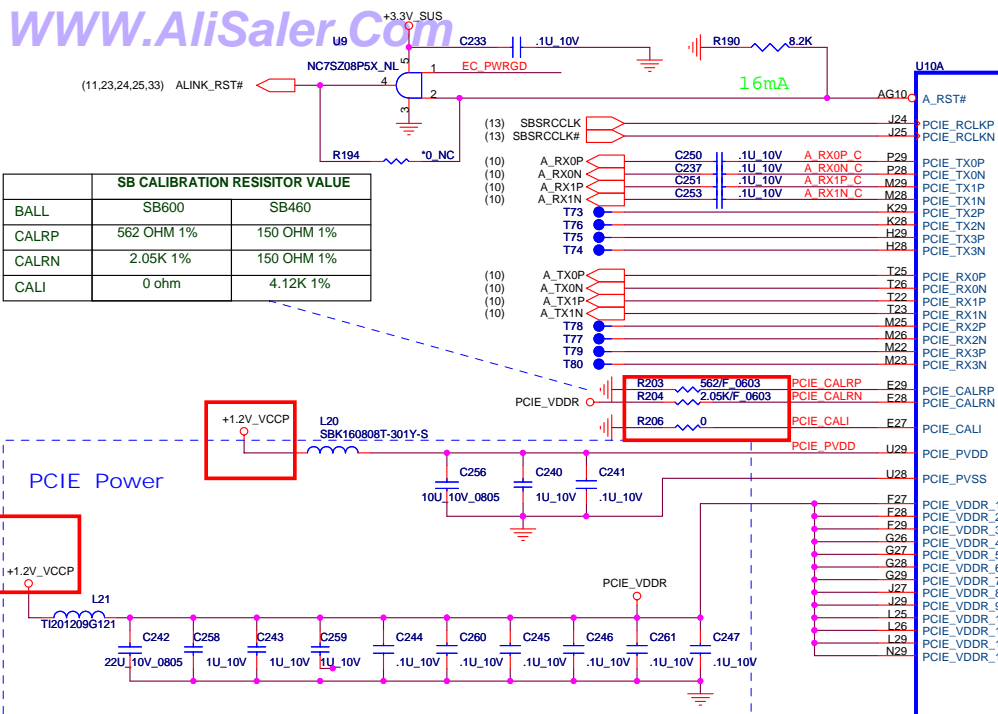
CLKREQA# CONTROL SRC5,6,7
CLKREQB# CONTROL SRC2,3,4, ATIG3
CLKREQC# CONTROL SRC0,1,ATIG0,1/2



QUANTA
COMPUTER

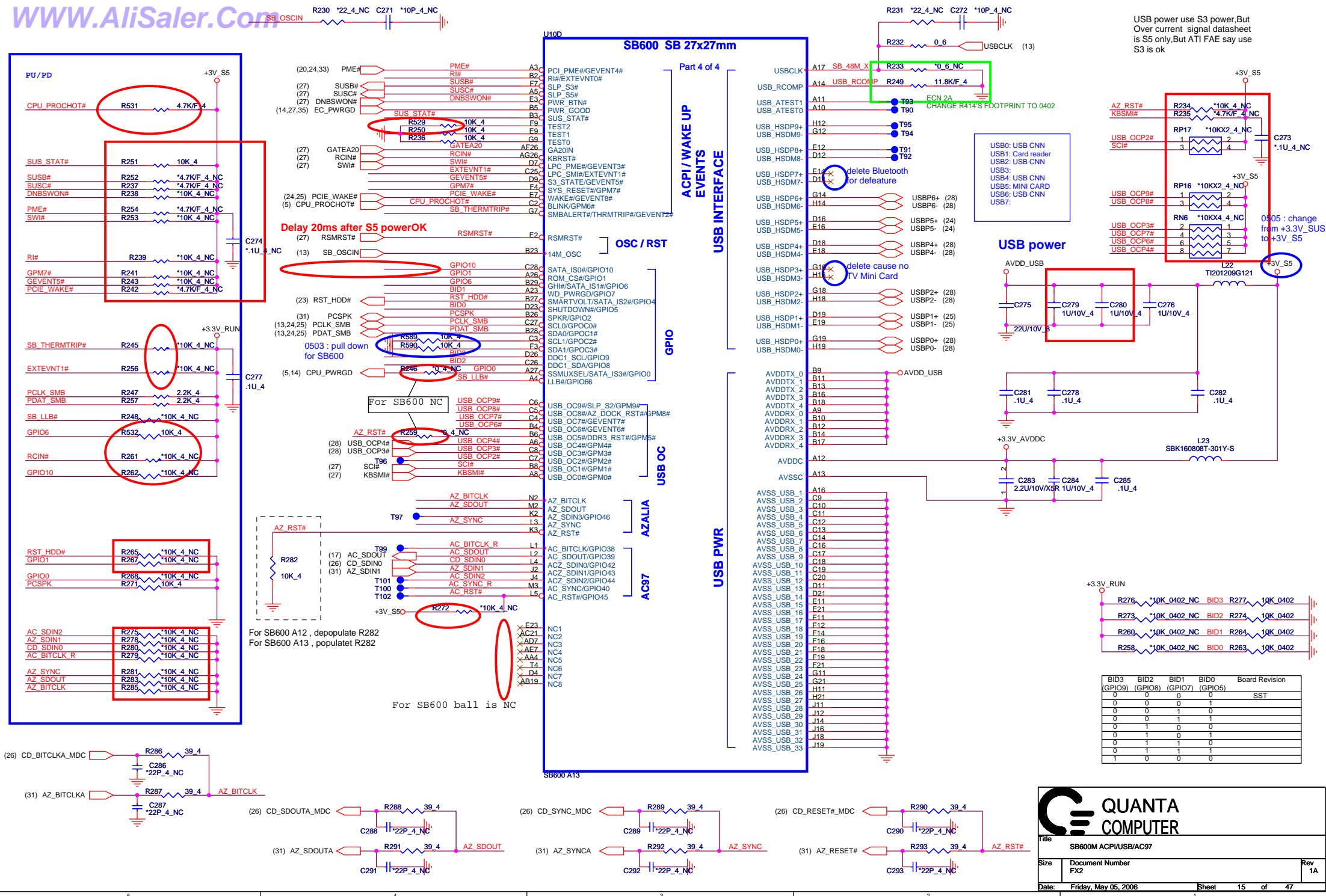
Title CLOCK GENERATOR		
Size FX2	Document Number FX2	Rev 1A
Date Friday, May 05, 2006	Sheet 13	of 47

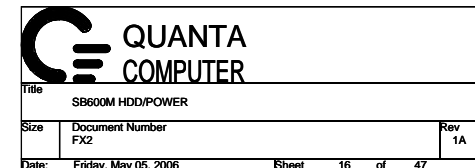
	SB CALIBRATION RESISTOR VALUE	
BALL	SB600	SB460
CALRP	562 OHM 1%	150 OHM 1%
CALRN	2.05K 1%	150 OHM 1%
CALI	0 ohm	4.12K 1%



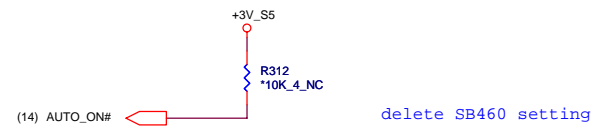
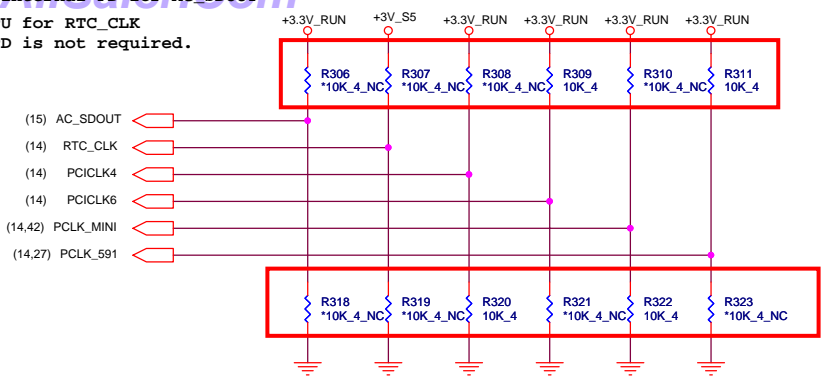
QUANTA
COMPUTER

Title		SB600M-PCIE/PC/MLPC	
Size	Document Number		Rev
	FX2		
Date	Friday, May 05, 2006	Sheet	14 of 47



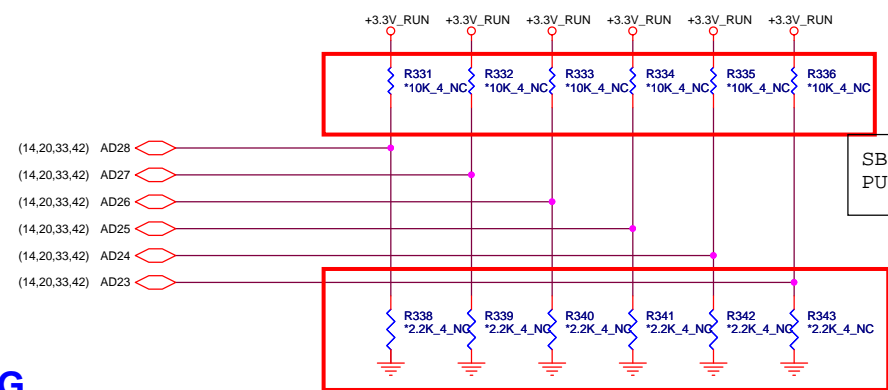
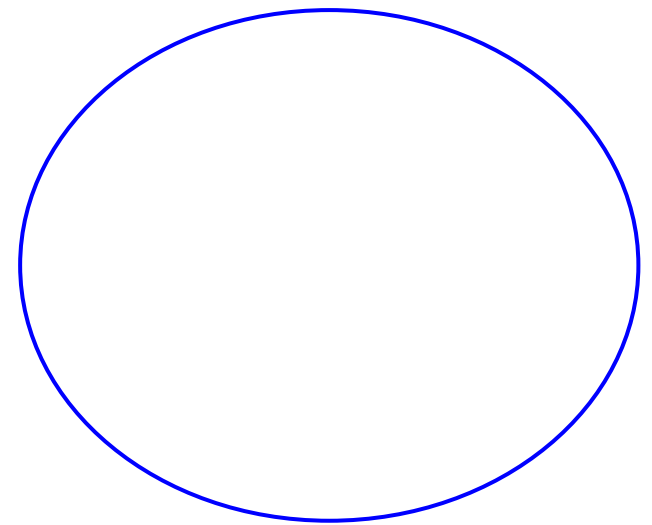


SB600 has 15K internal PU for AC_SDOUT
15K internal PU for RTC_CLK
,External PU/PD is not required.



REQUIRED STRAPS

						PCLK_MINI	PCLK_591
PULL HIGH	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1	
	USE DEBUG STRAPS	INTERNAL RTC	USE INT. PLL48	CPU IF=K8	H, H = PCI ROM H, L = SPI ROM		
PULL LOW	IGNORE DEBUG STRAPS	EXTERNAL RTC	USE EXT. 48MHZ	CPU IF=P4	L, H = LPC ROM L, L = FWH ROM	DEFAULT	



SB600 HAS 15K INTERNAL PU FOR PCI_AD[28:23]


DEBUG STRAPS

	PDACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET	Use Long Reset	USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	boot fail time disabled
PULL LOW	USE SHORT RESET	Use Short Reset	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	boot fail time enabled

SB460 Only

SB600 Only

SB600 Only

**QUANTA
COMPUTER**

TitleSB600M STRAPS

SizeDocument NumberFX2Rev1A

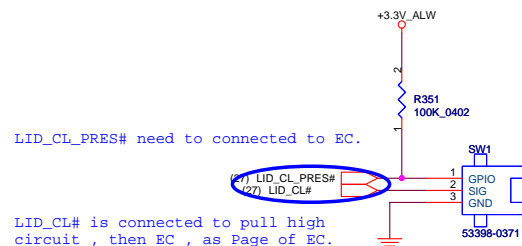
Date:Friday, May 05, 2006Sheet17 of 47

change name as ED5 SB.

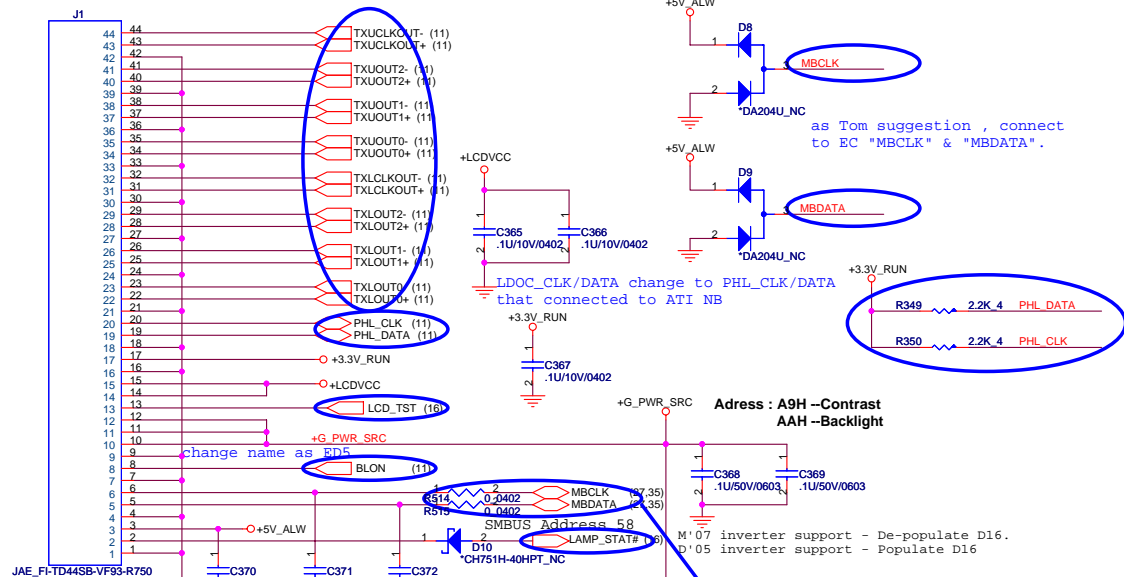


LID_CL_PRES# need to connected to EC.

LID_CL# is connected to pull high circuit, then EC, as Page of EC.



change name as ED5 SB.



For Discrete:
De-populate J1, R230, C311, C331, C332, D16, C333, C329, C341, C324, C326

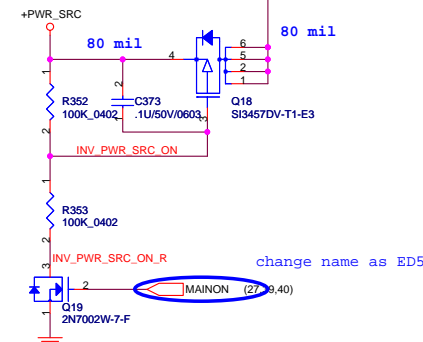
On FM1, LCD_TST & LAMP_STAT connect to SB ; on FX2 ??.

as Tom suggestion, connect to EC "MBCLK" & "MBDATA".

Adress : A9H --Contrast
AAH --Backlight

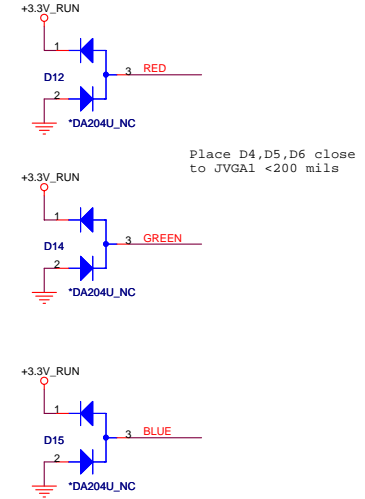
M'07 inverter support - De-populate D16.
D'05 inverter support - Populate D16.

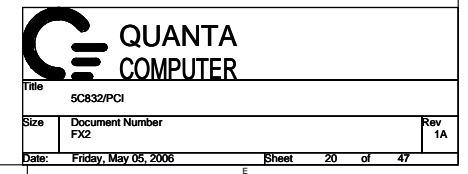
as Tom suggestion, connect to EC "MBCLK" & "MBDATA".

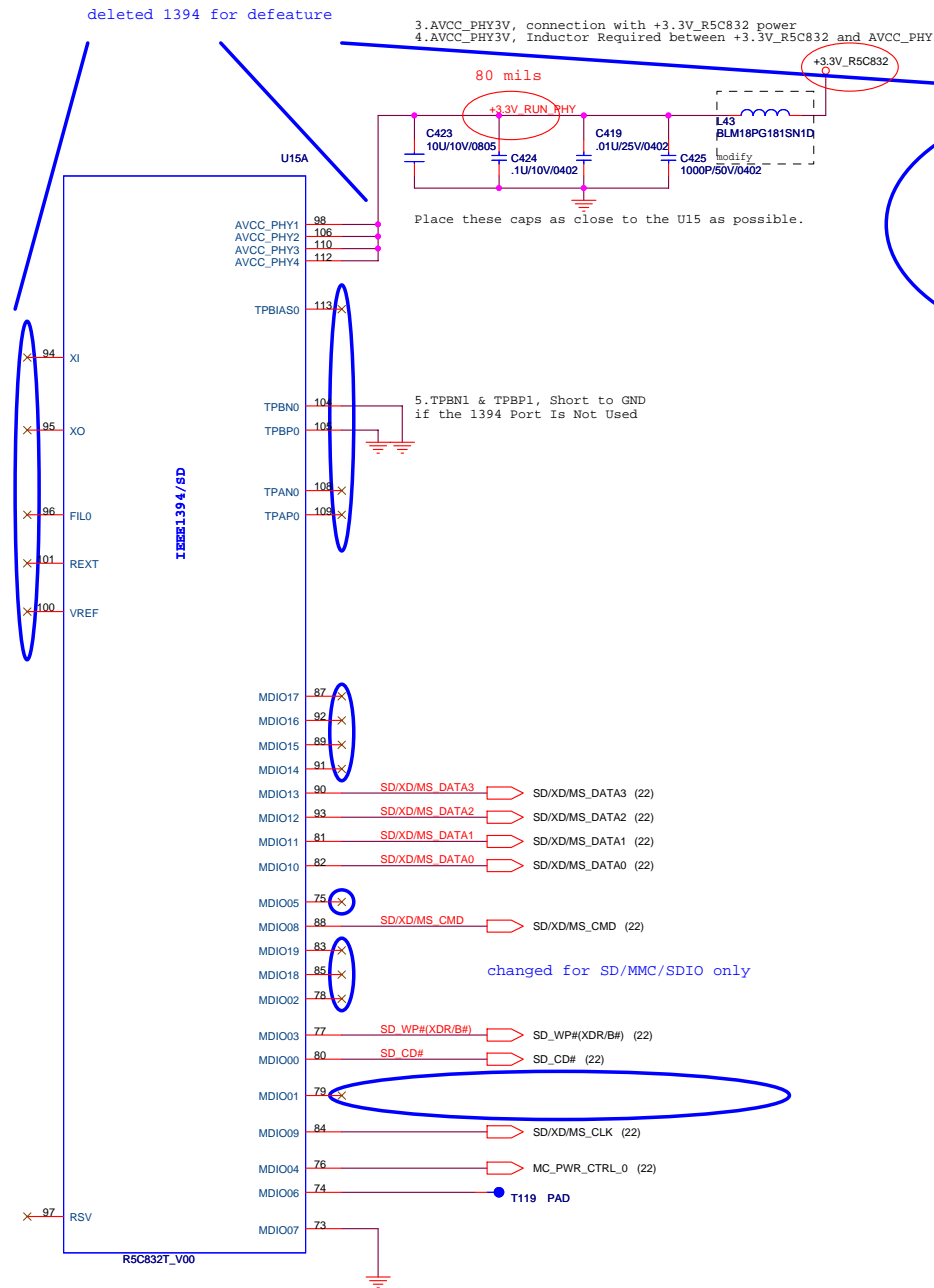


Title			LCD CONN
Size	Document Number	Rev	
	FX2	1A	
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```
delete Svideo for defeature
```

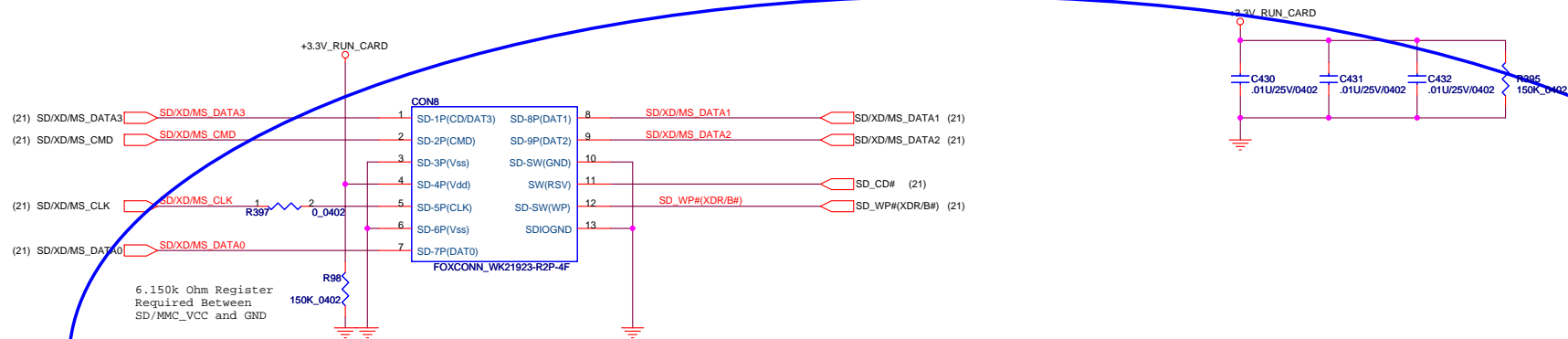




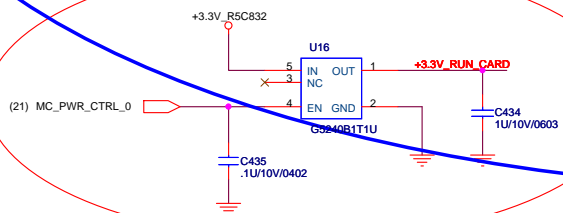


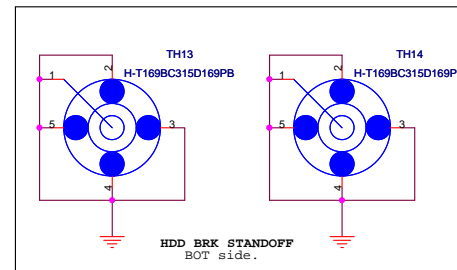
DO NOT INSERT SD/MMC SIMULTANEOUSLY.

changed for SD/MMC/SDIO only



For SD/MS power





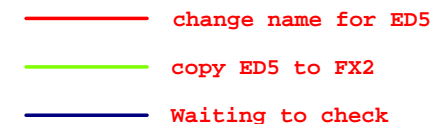
SATA RX0- C 2 | 1 3900P/25V/0402 SATA_RXN0 (16)
C436

SATA RX0+ C 2 | 1 3900P/25V/0402 SATA_RXP0 (16)
C437

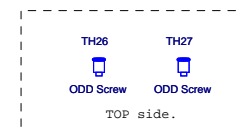
Locate caps C558, C559 near HDD Conn.
Length match SATA_C_RX0- & SATA_C_RX0+ within 20mils.

SATA drive vendors will use only 5V supply from the system and will derive 3.3V on the drive. If drive power goals are not achieved, drive vendors will use both 5V and 3.3V supplies from the system. Initial power saving using 3.3V from system is less than 5%.

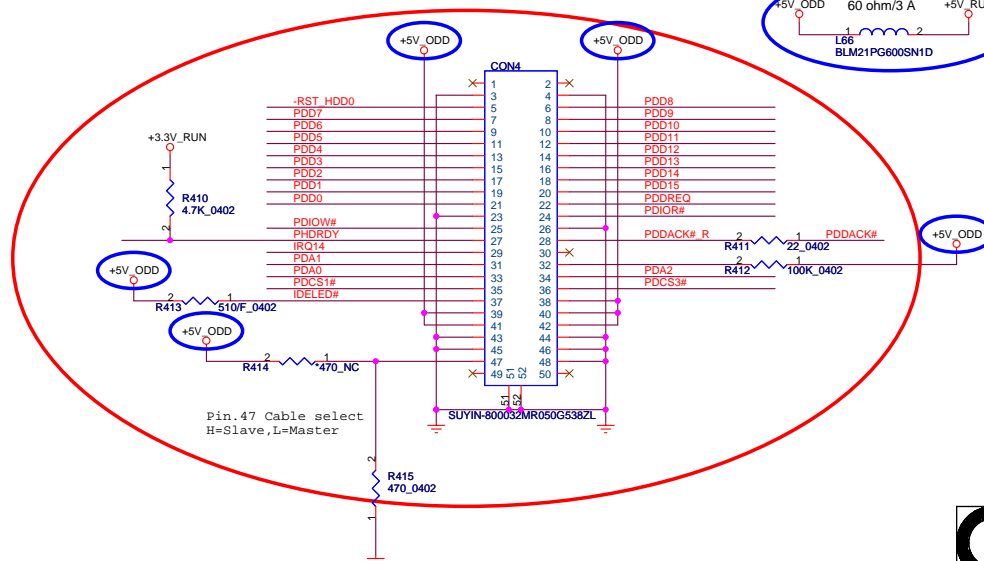
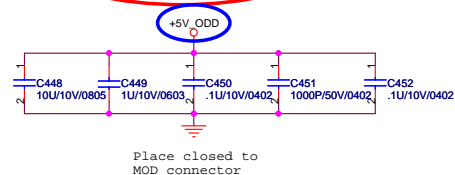
Power Estimate:
SATA drive power consumption estimate at
MobileMark is 1.1W. An additional 150mW
can be saved using Intel's IMST driver.



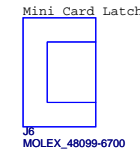
0502 : reserve L66 for current measurement , can be removed and short directly after RTS ; and change +5V_RUN to +5V_ODD for ODD side power



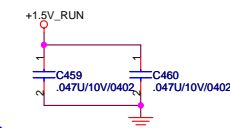
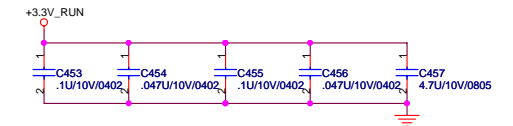
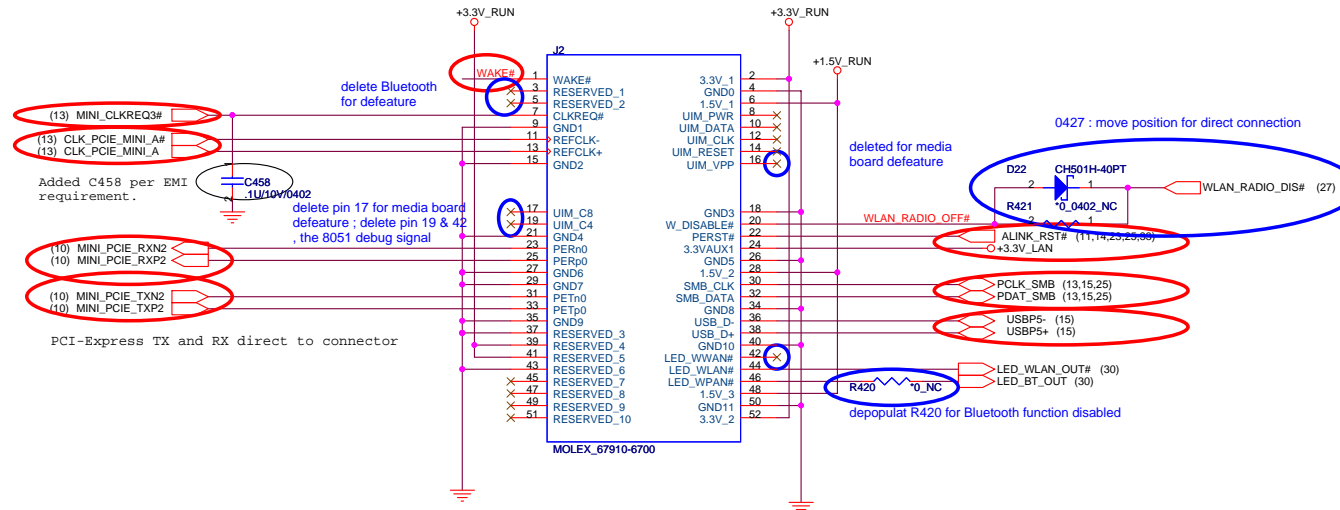
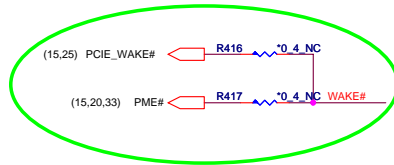
PATA ODD



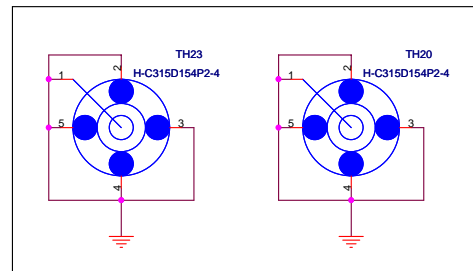
MINI CARD



- change name for ED5
- copy ED5 to FX2
- Waiting to check



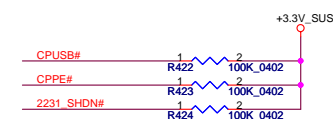
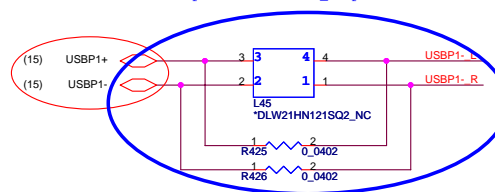
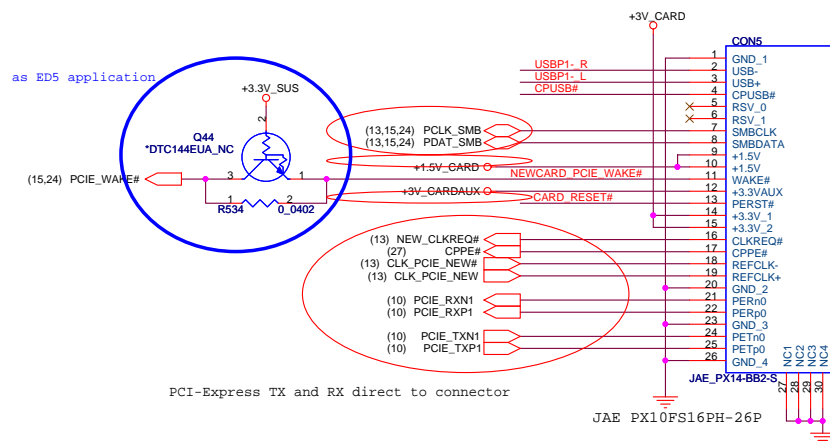
Express Card



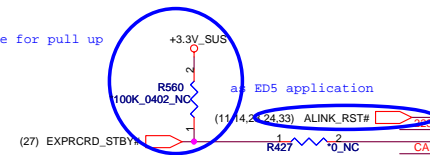
- change name for ED5
- copy ED5 to FX2
- Waiting to check

NEW CARD GUIDE POST
TOP side.

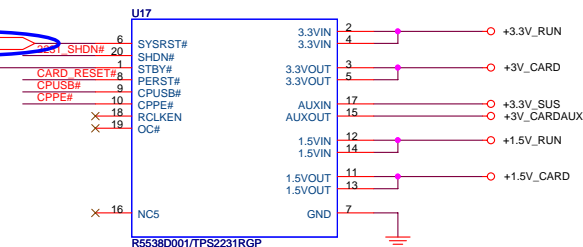
swap traces as "fx2_swap-0412"



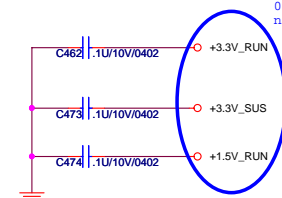
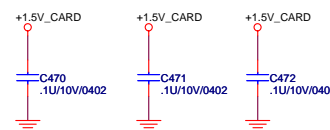
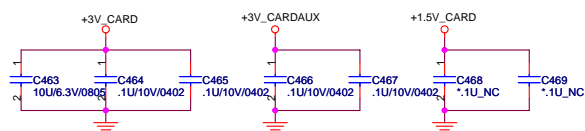
reserve for pull up



+1.5V_CARD Max. 650mA, Average 500mA
+3V_CARD Max. 1300mA, Average 1000mA



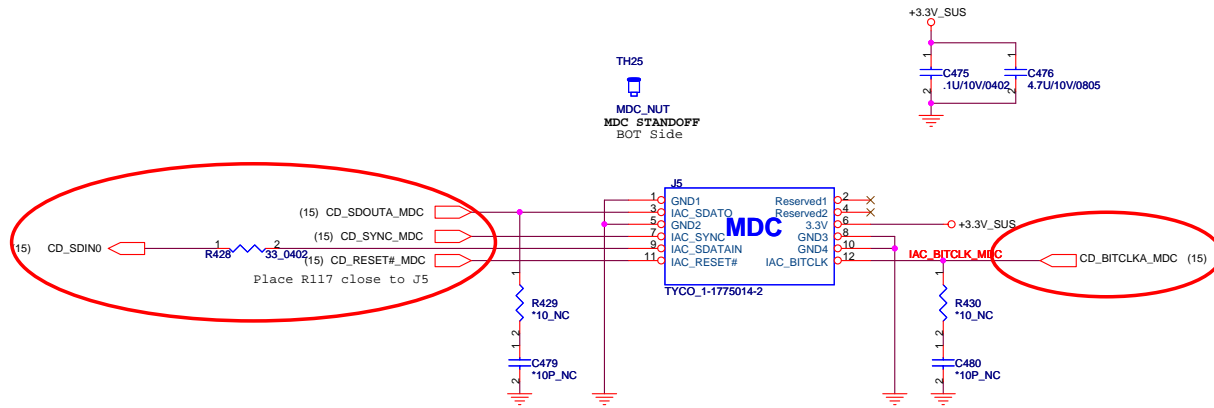
+1.5V_CARD Max. 650mA, Average 500mA
+3V_CARD Max. 1300mA, Average 1000mA



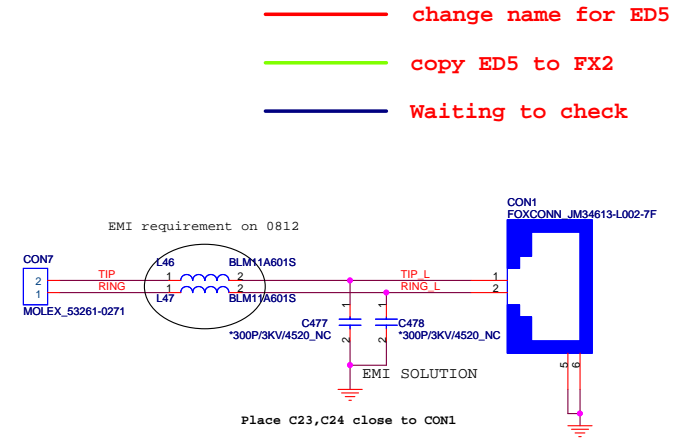
0427 : change from only net
name to symbol "power point"

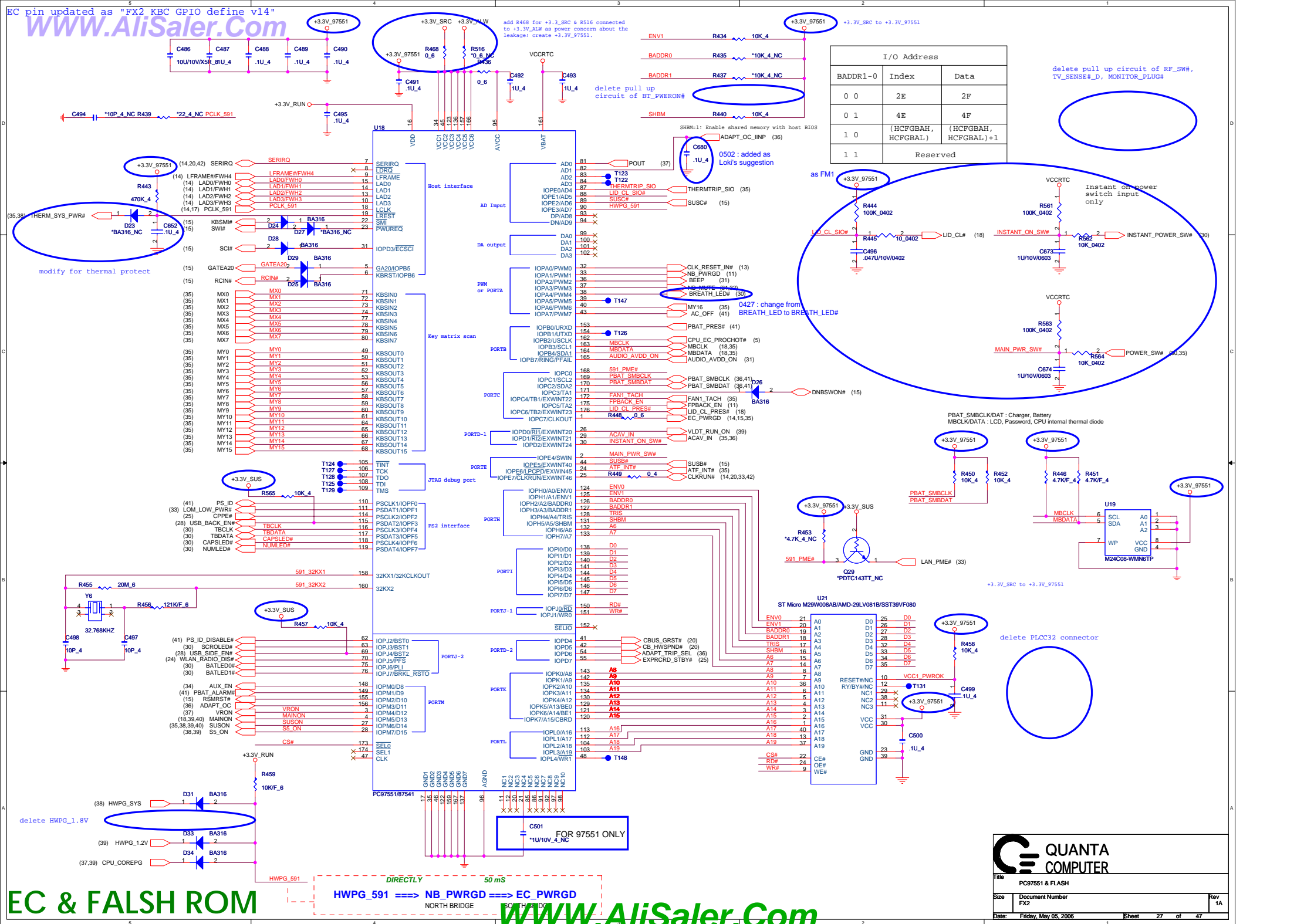
QUANTA COMPUTER	
Title: Express Card	
Size: Document Number FX2	Rev: 1A
Date: Friday, May 05, 2006	Sheet: 25 of 47

1. Tip and Ring trace width = 25 mils
2. Spacing between Tip and Ring = 25 mils
3. Tip and Ring connector pitch = 25 mils
4. Keep out area from Tip and Ring to other signals = 100 mils
5. Power and Ground minimum trace width to connector = 20 mils
6. Route Tip and Ring on one layer only (top or bottom)
7. Modem internal cable wire size = 26 AWG
(stranded or twisted pair wire)



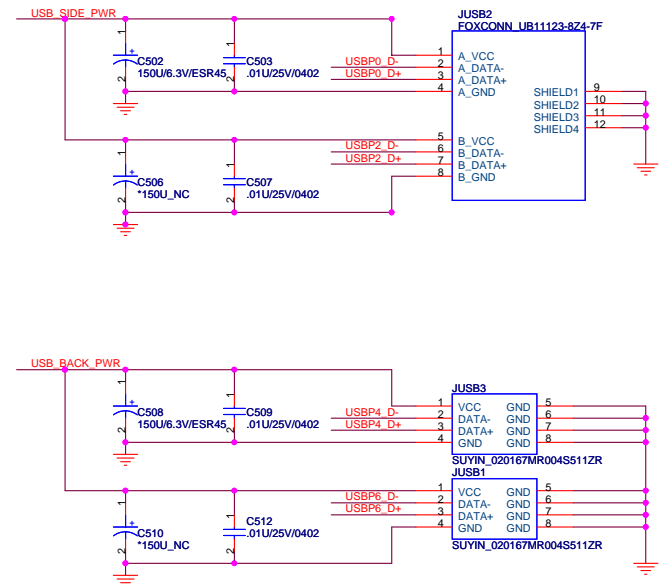
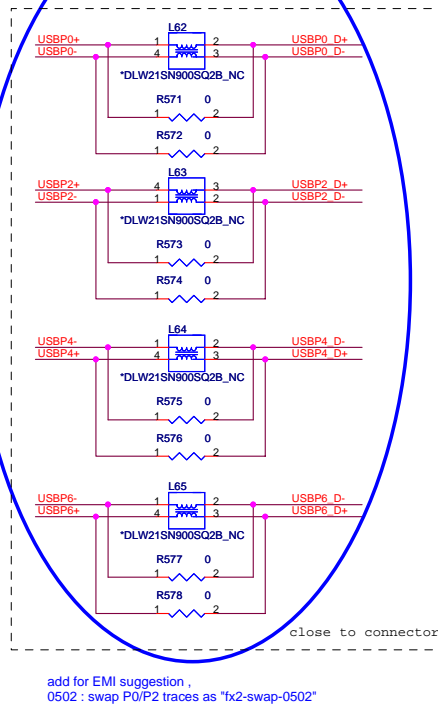
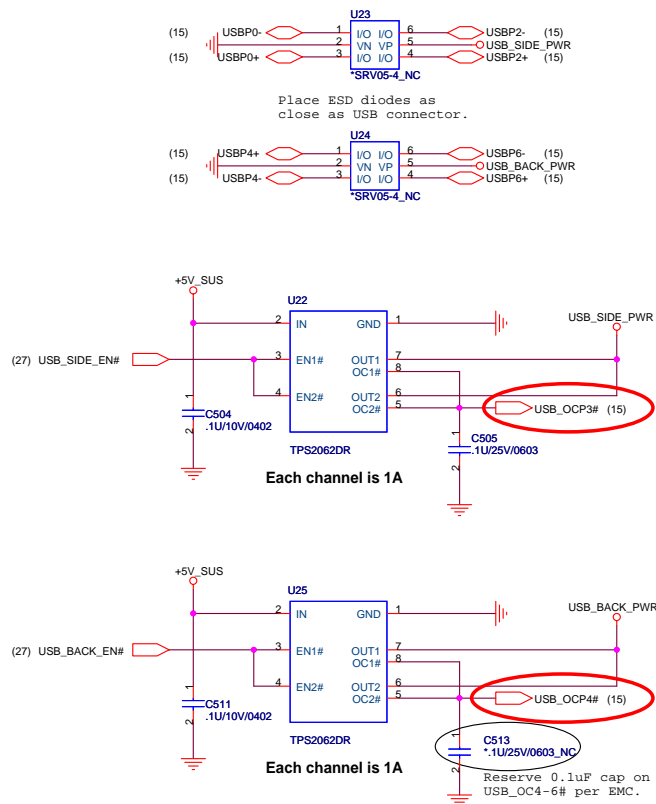
```
delete Bluetooth
for defeature
```

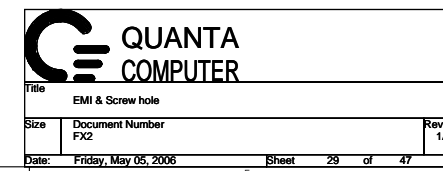


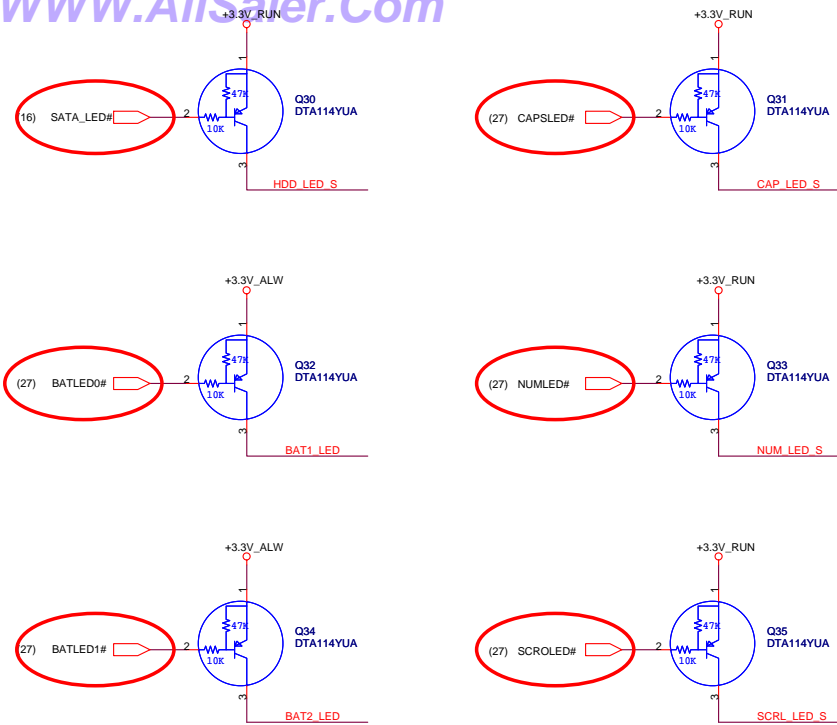


8Mbit (1M Byte), SPI

- change name for ED5
- copy ED5 to FX2
- Waiting to check

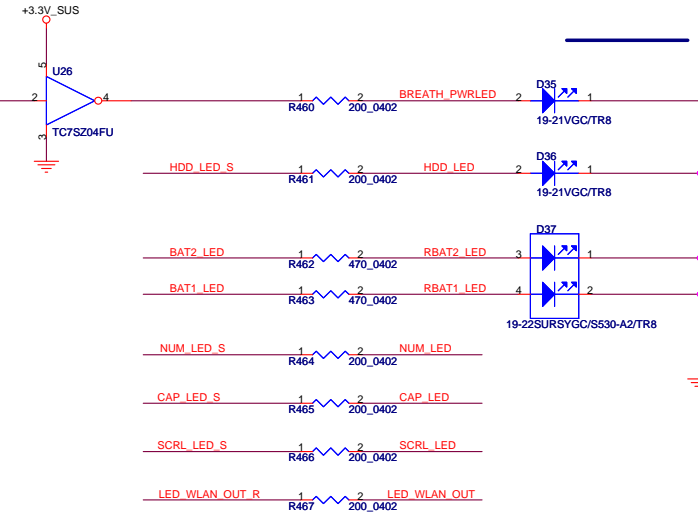




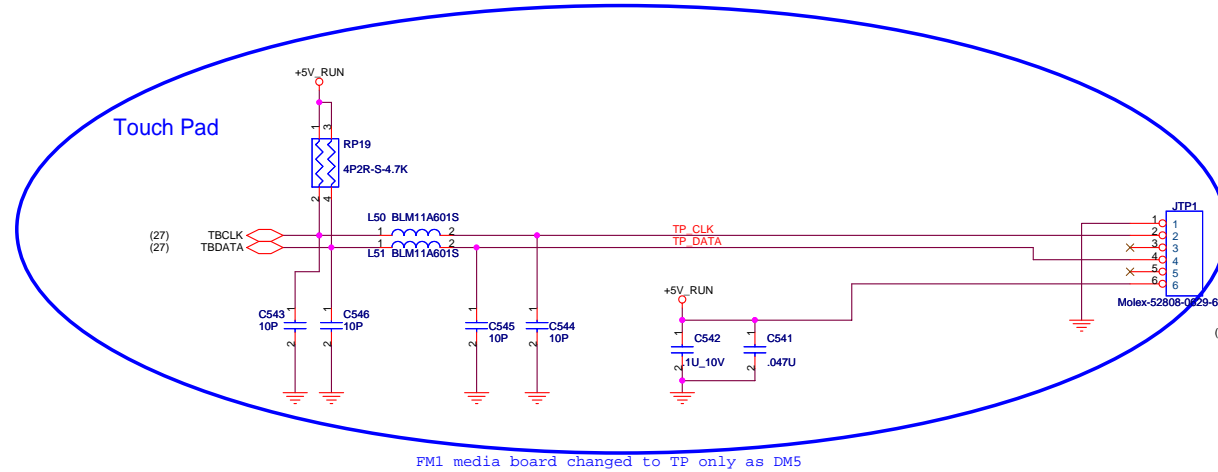


0427 : change from
BREATH_LED to BREATH_LED#

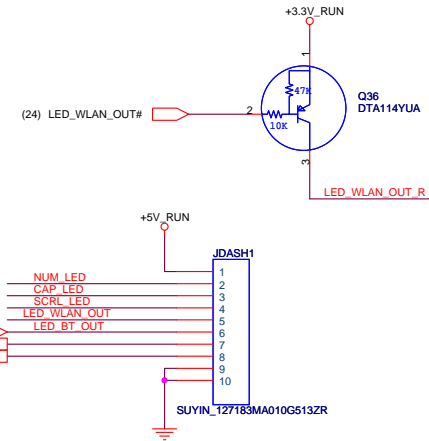
(27) BREATH_LED#



change name for ED5
copy ED5 to FX2
Waiting to check



FM1 media board changed to TP only as DM5



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COMPUTER

SWITCH & TP & LED

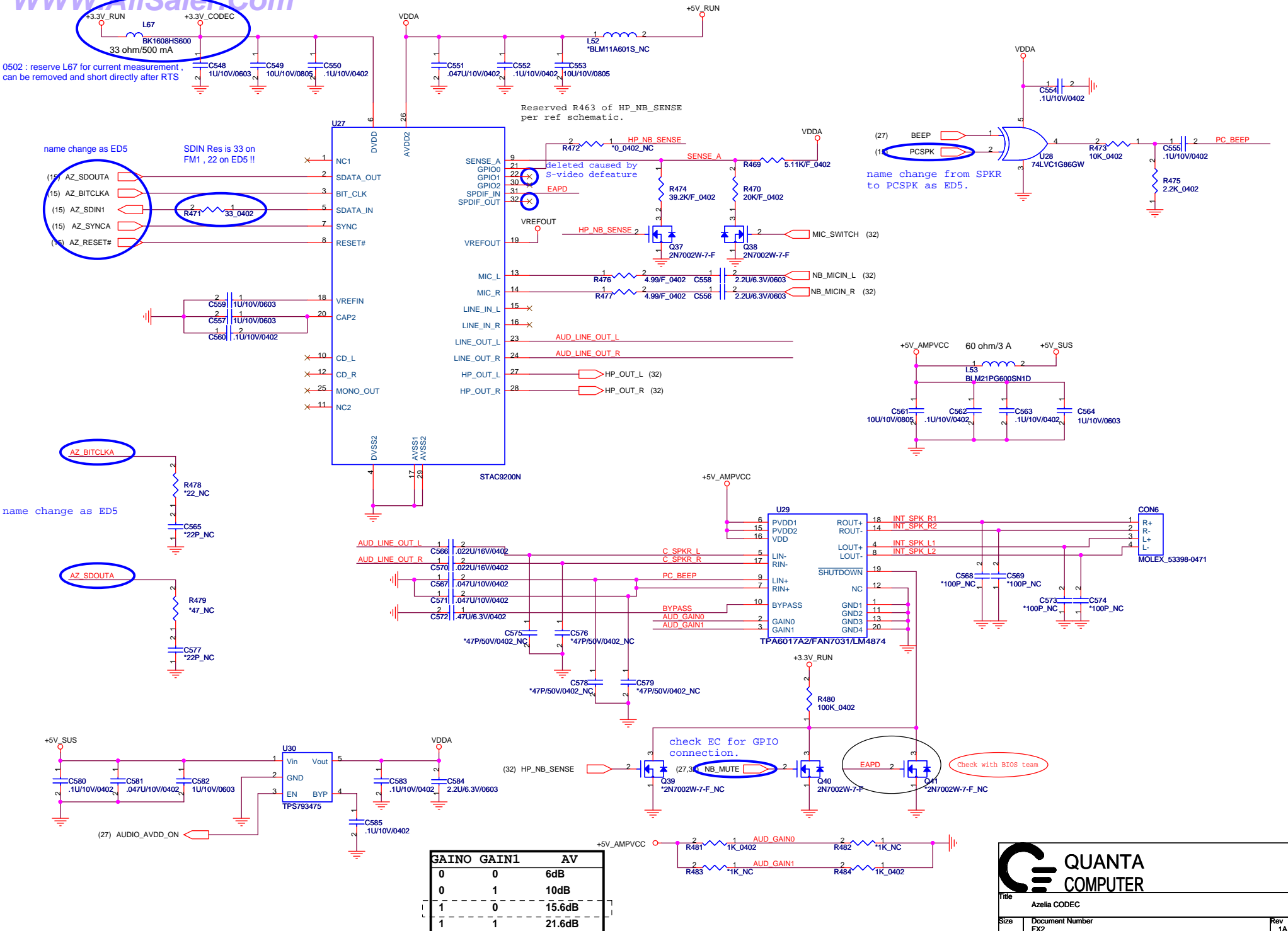
Size Document Number

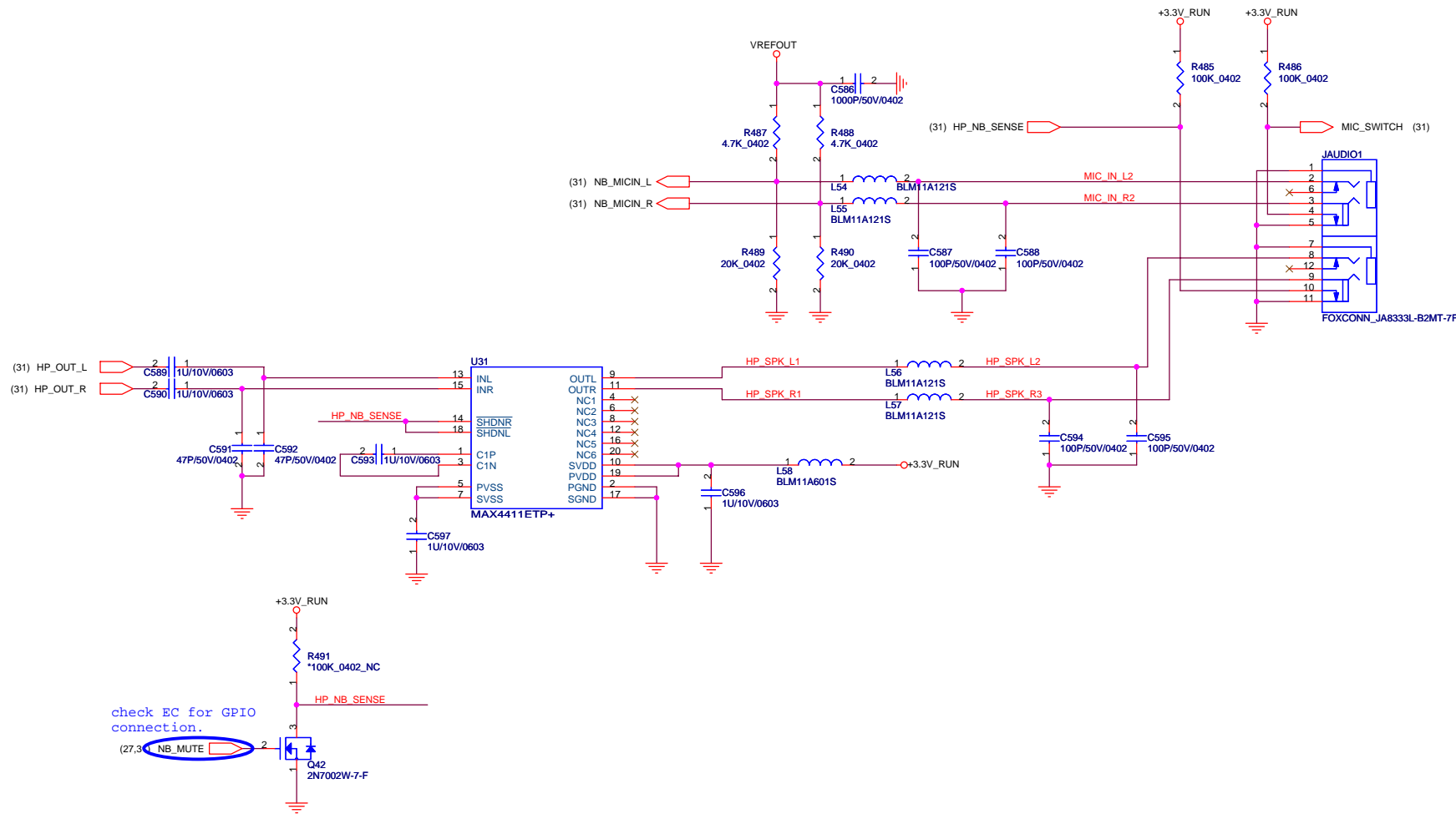
FX2


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Title AUDIO CONN		
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Close to power pins
0.1U*13 pcs

Place C607 close to pin65

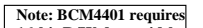
EMI requirement on 0812

These three pin
LINK_LED10#,
LINK_LED100#,
ACT_LED are
open-drain type.

change name for ED5

copy ED5 to FX2

Waiting to check



Note: The BCM4401 has weak internal pulldown resistors on the following signals:
SPROM_CS, SPROM_CLK, SPROM_DOUT, SPROM_DIN.

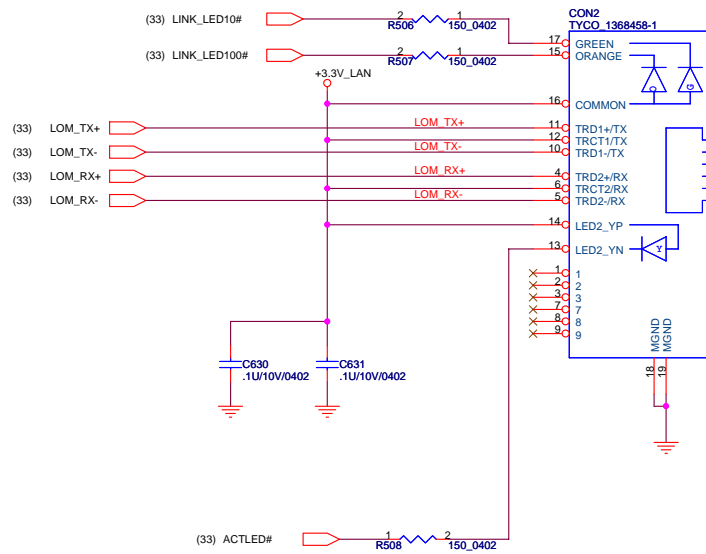


Title	LAN(BCM4401)
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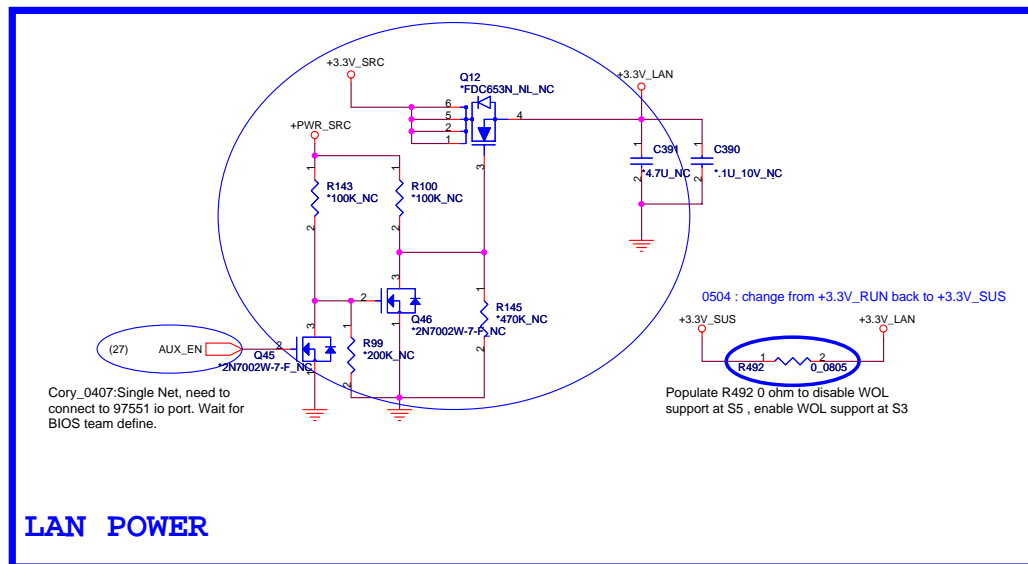
Size	Document Number FX2
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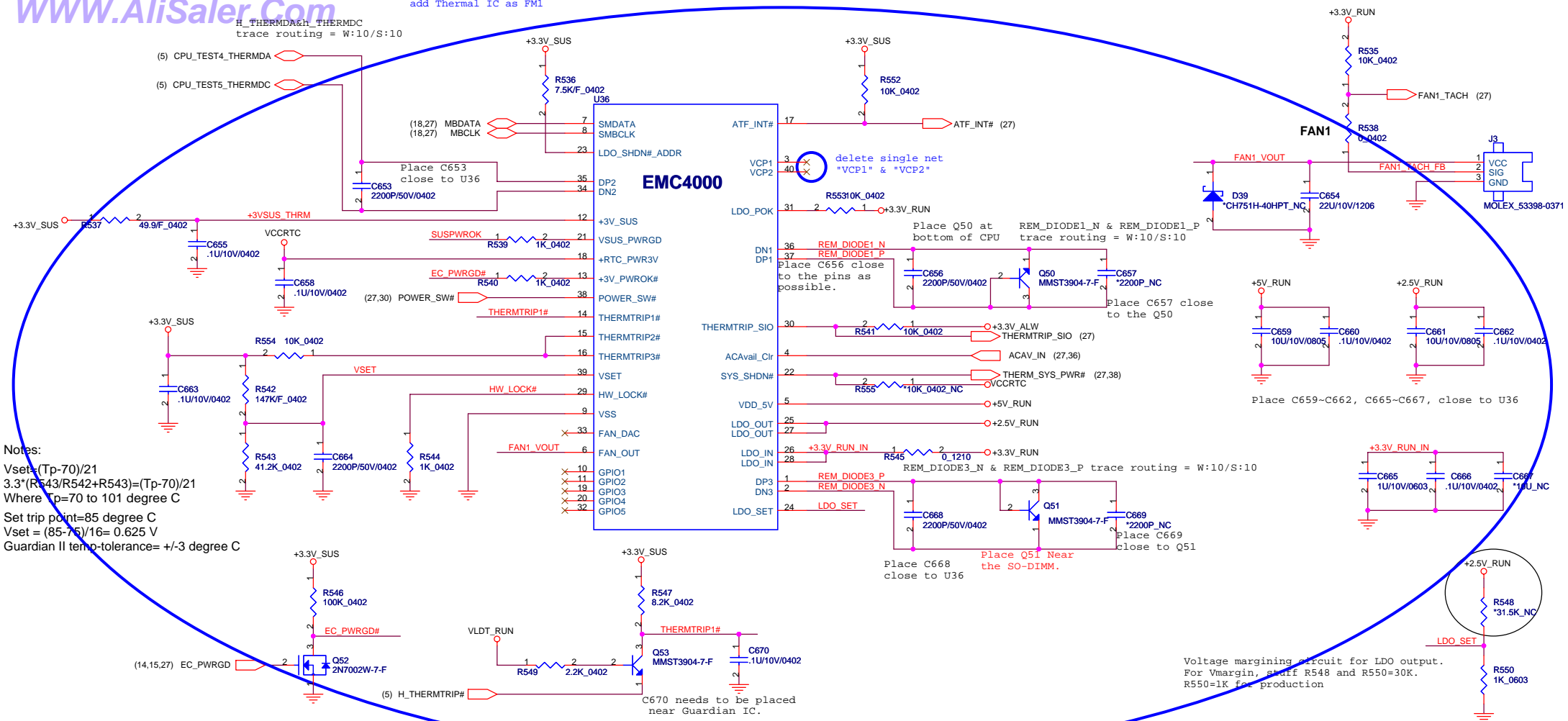
Date: Friday, May 05, 2006

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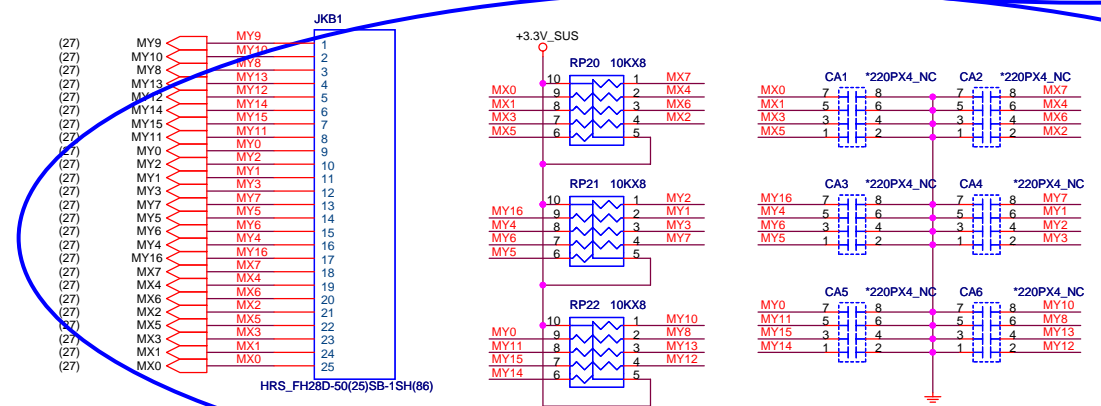
- change name for ED5
- copy ED5 to FX2
- Waiting to check
- copy DM5 to FX2



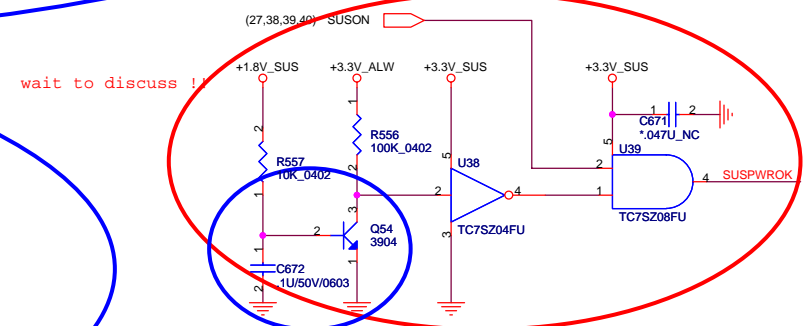


Notes:
 $V_{set} = (T_p - 70) / 21$
 $3.3 \cdot (R_{43} / R_{542} + R_{543}) = (T_p - 70) / 21$
 Where $T_p = 70$ to 101 degree C
 Set trip point = 85 degree C
 $V_{set} = (85 - 76) / 16 = 0.625$ V
 Guardian II temp-tolerance = ± 3 degree C

as FM1 keyboard matrix & "e0788.1104a_swap-0422"



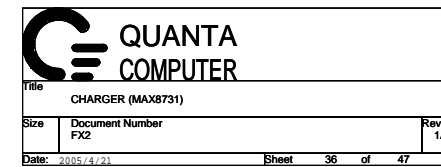
KBC

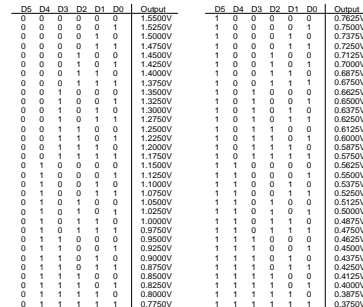


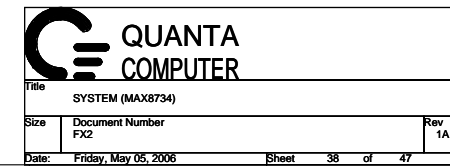
0427 : change Q54 from 2N7002W-7-F to 3904 ; C672 from .1U/10V/0402 to .1U/50V/0603 as voltage level & timing concern

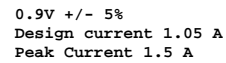
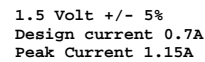
QUANTA
COMPUTER

Title KB & THERMAL & FAN		
Size FX2	Document Number FX2	Rev 1A
Date Friday, May 05, 2006	Sheet 35	of 47

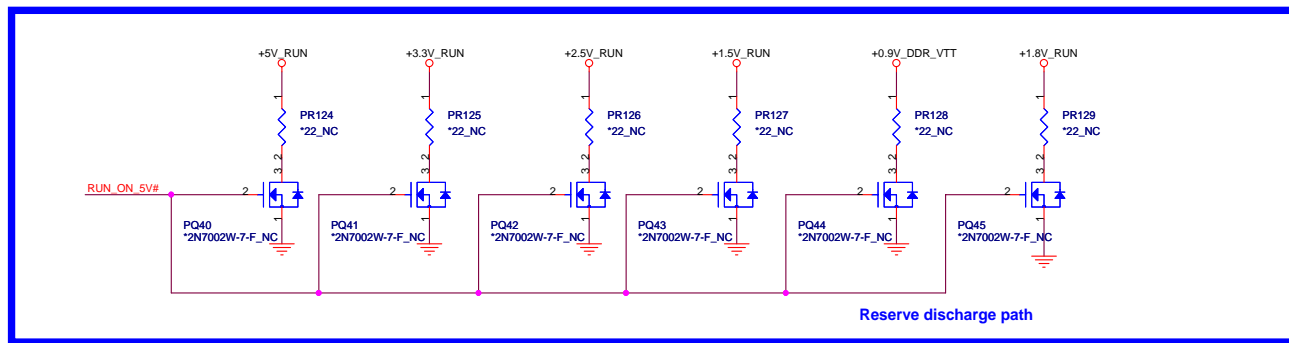
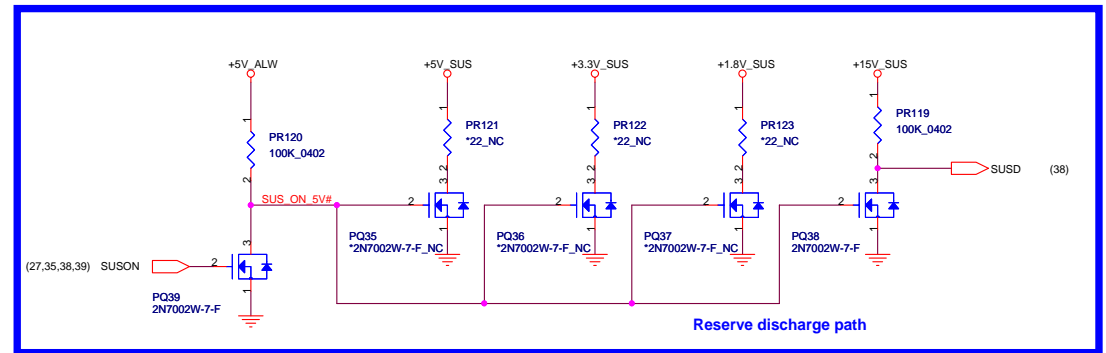
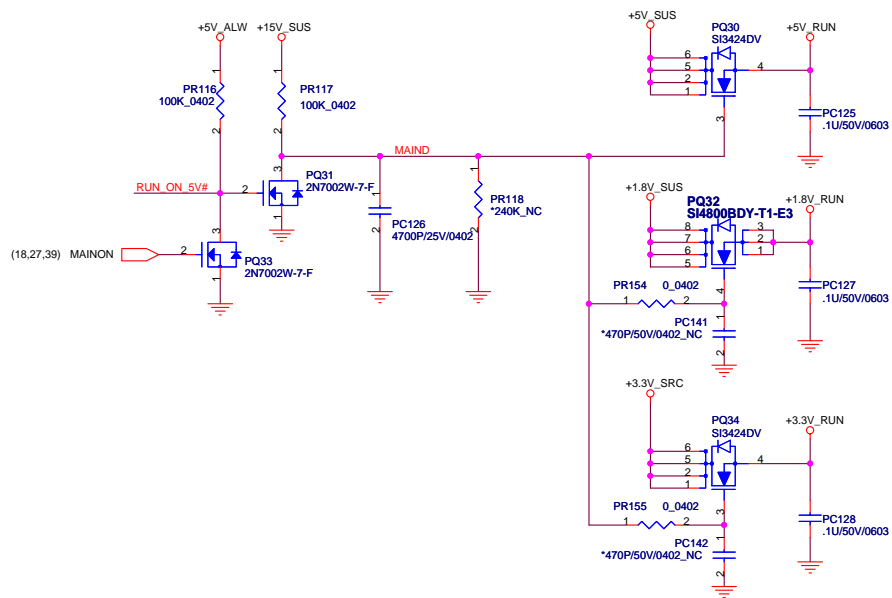





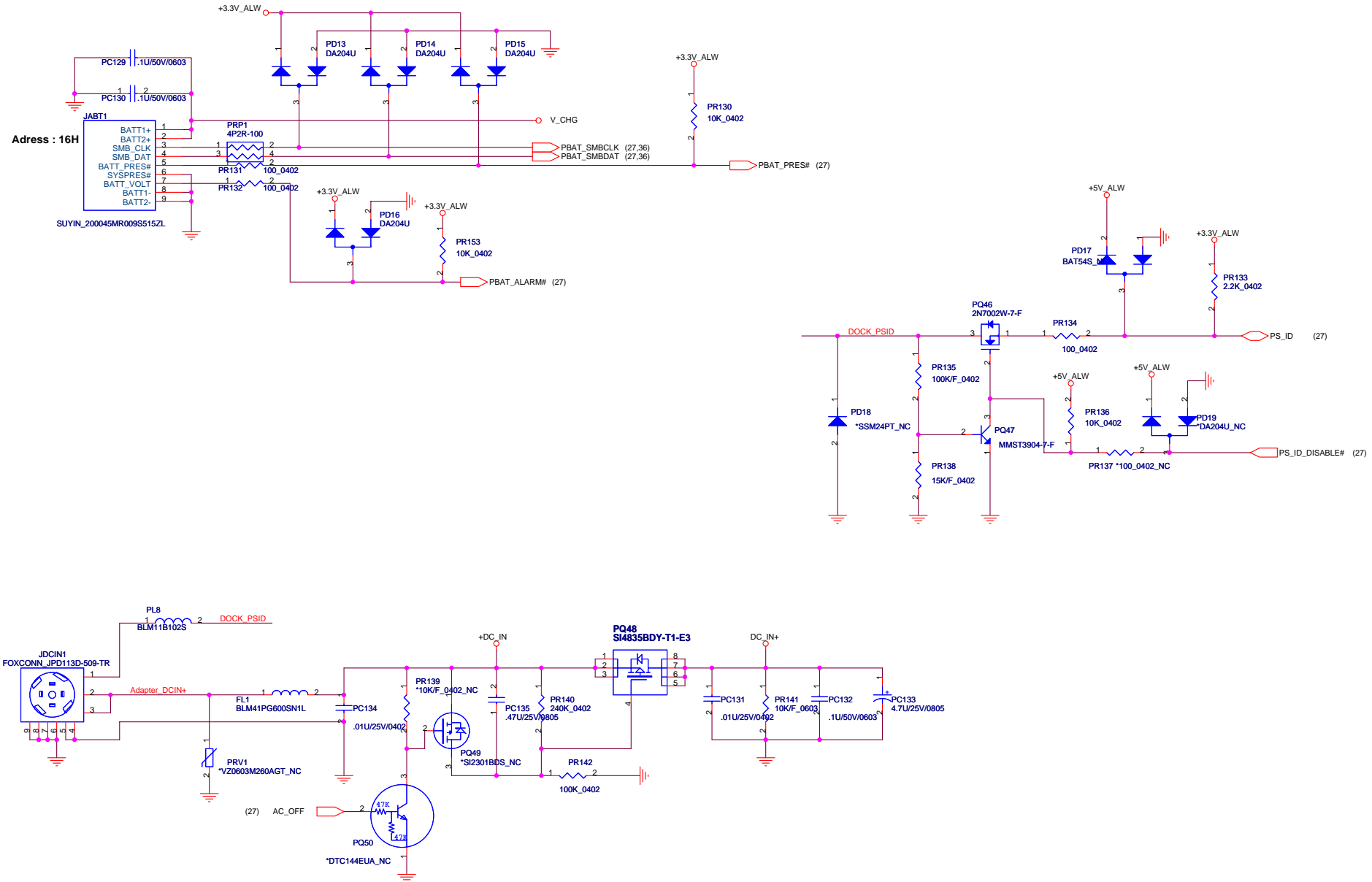




Title			
VCCP			
Size	Document Number		Rev
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Date:	2005/4/21	Sheet	39 of 47

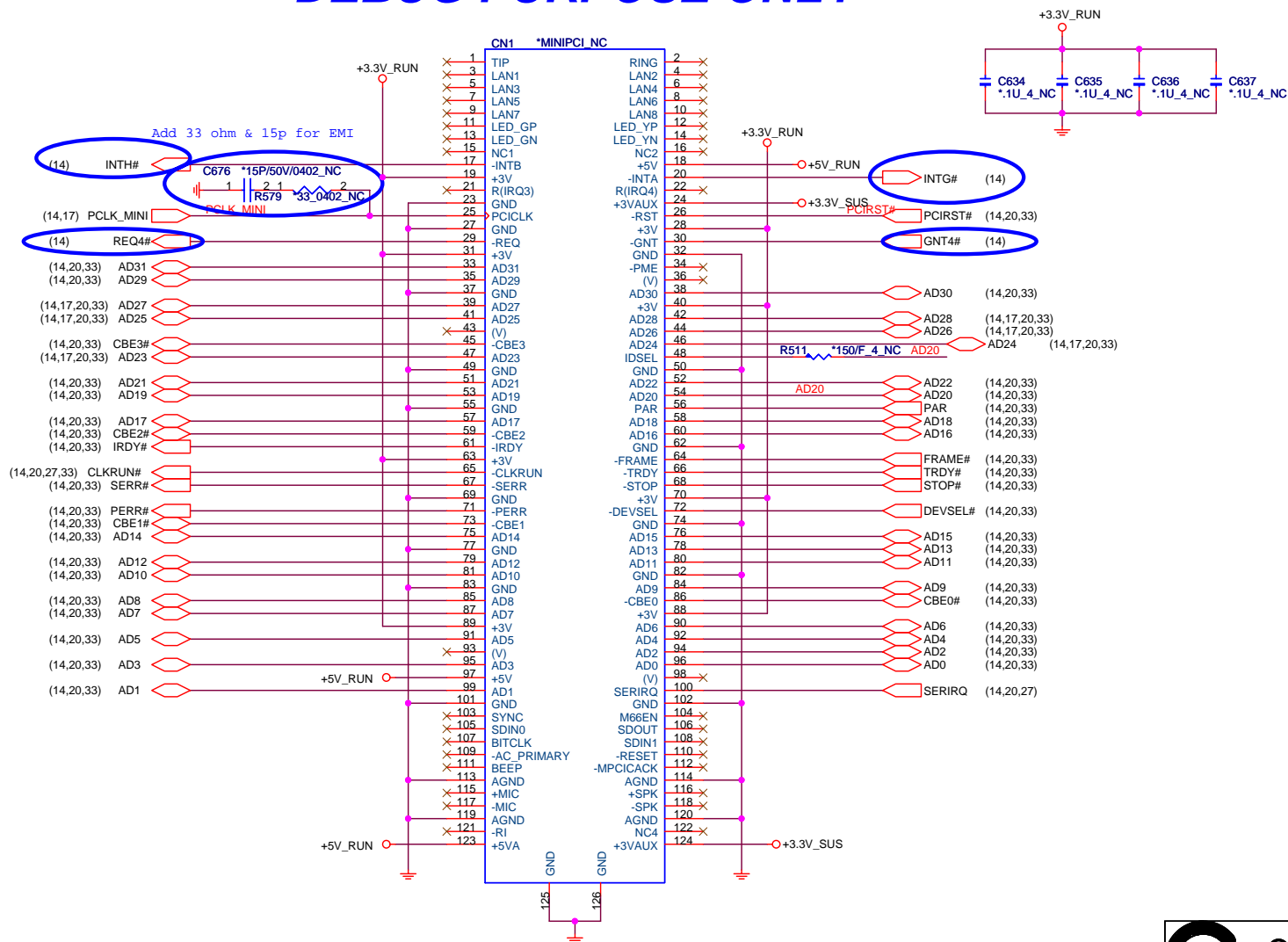


 QUANTA COMPUTER		
Title	RUN POWER SW	
Size	Document Number FX2	Rev 1A
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QUANTA COMPUTER	
Title	DCIN,Batt
Size	Document Number FX2
Date:	Friday, May 05, 2006
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DEBUG PURPOSE ONLY



QUANTA COMPUTER

Title	MINI PCI(for debug)
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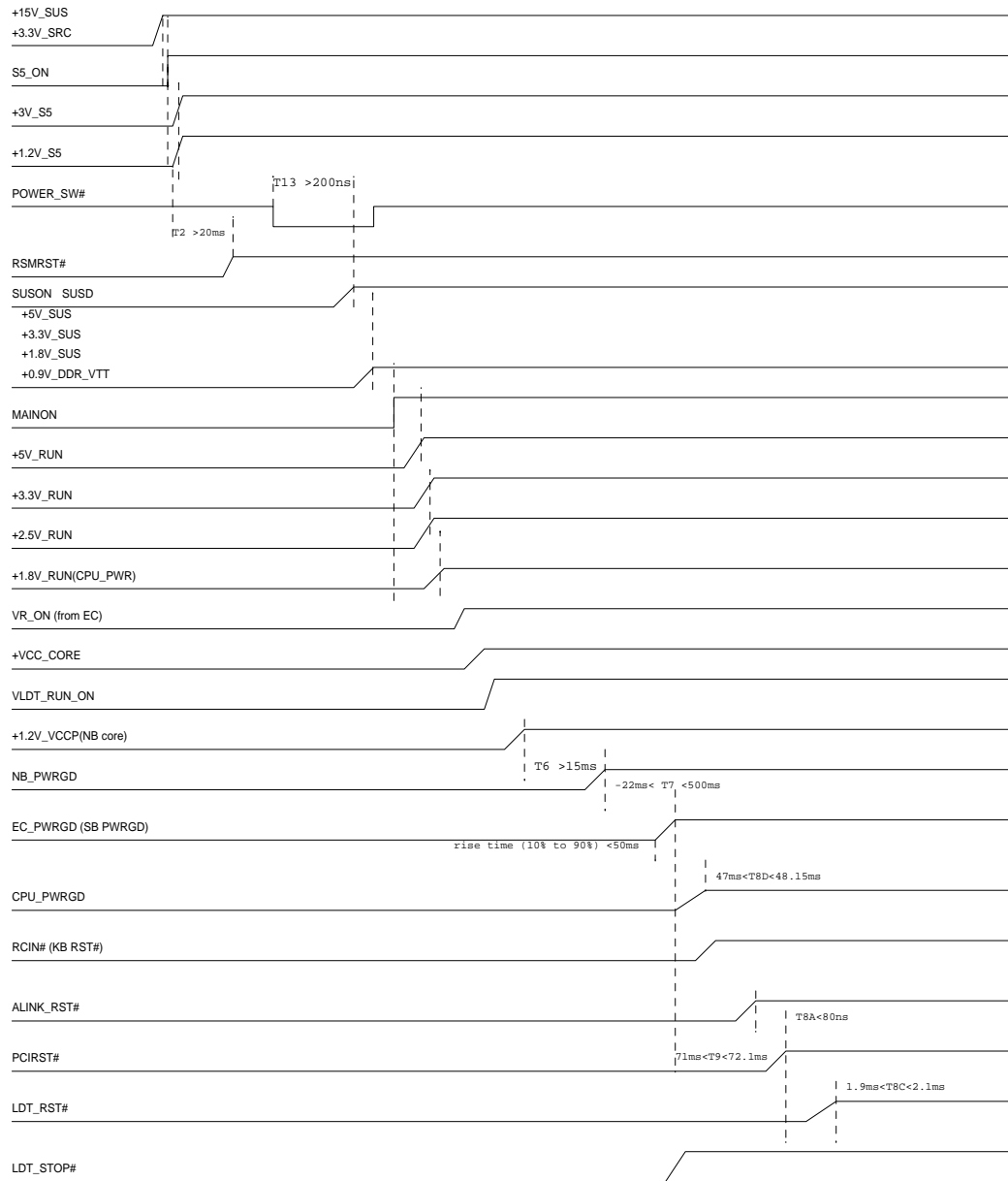
Size	Document Number FX2
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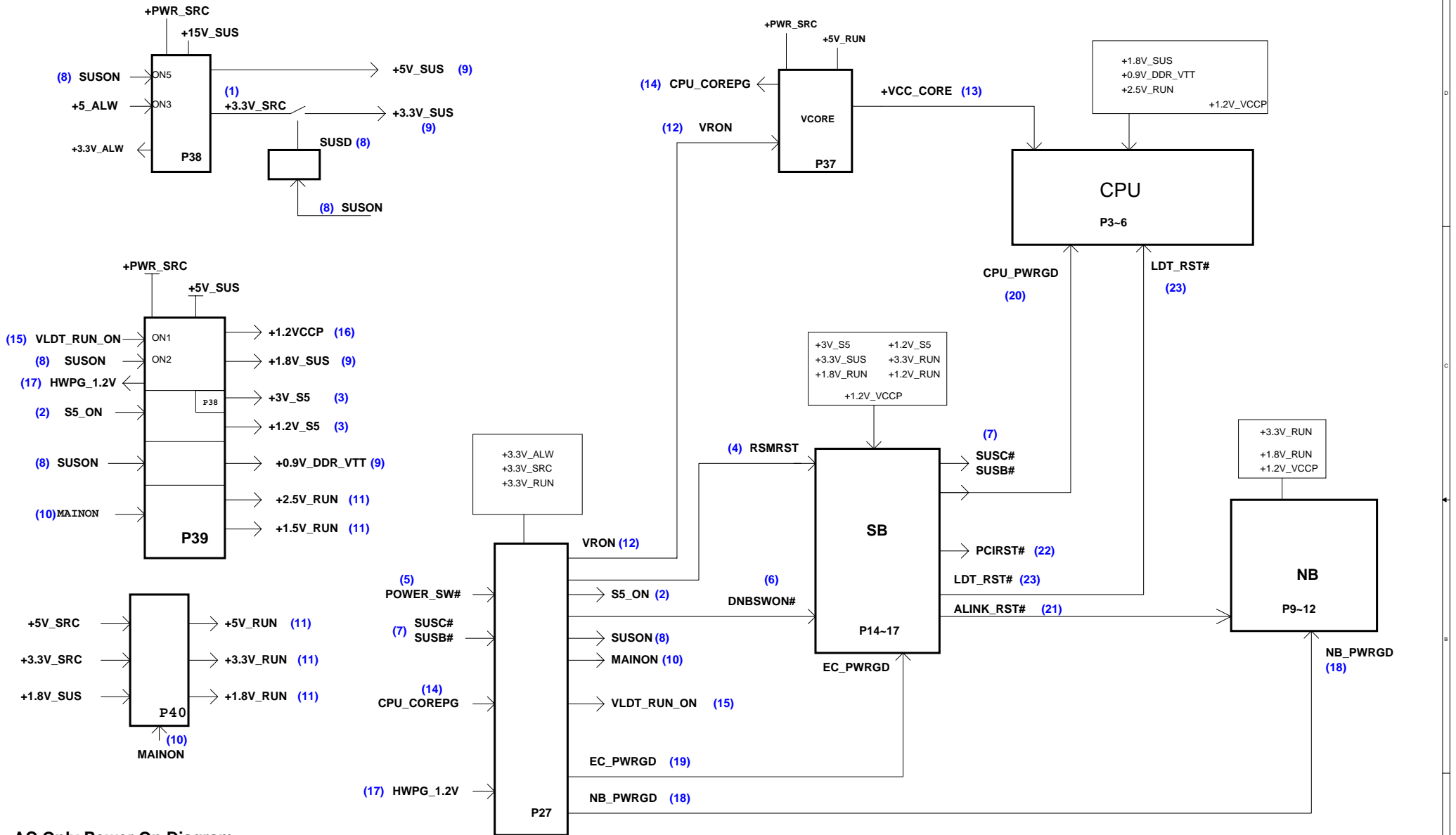
Power On Sequence



T6: NB core voltage to NB_PWRGD
T7: NB_PWRGD to SB_PWRGD
T8D: SB_PWRGD to CPU_PWRGD

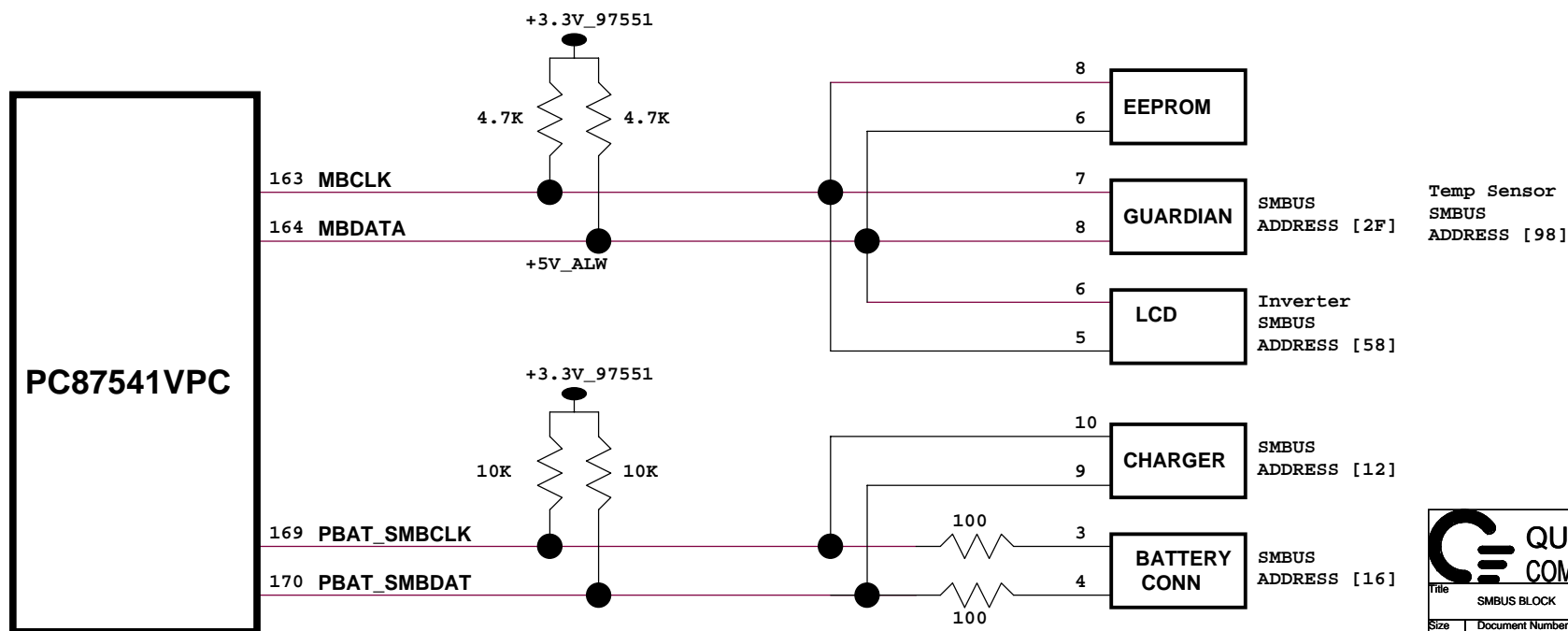
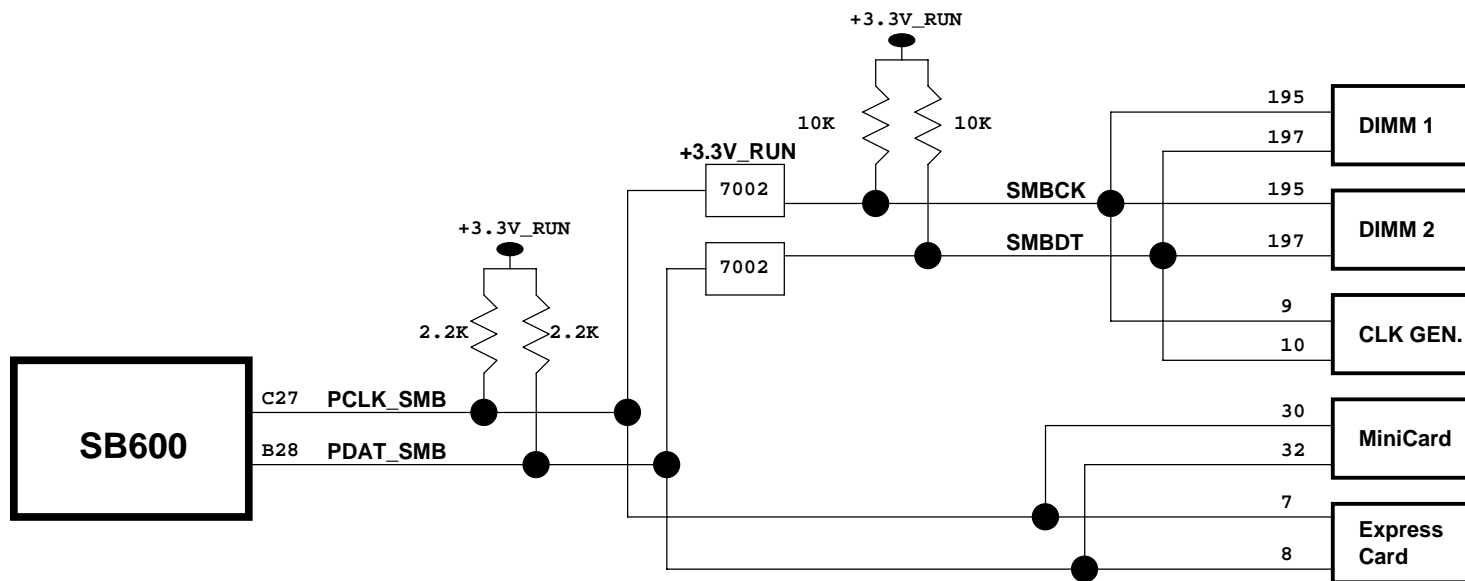
T8A: ALINK_RST# to PCIRST#
T9: SB_PWRGD to PCIRST#
T8C: PCIRST# to LDT_RST#


QUANTA COMPUTER	
File Power On Sequence	
Size	Document Number FX2
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AC Only Power On Diagram

(1) +3.3V_SRC	(8) SUSON, SUSD	(13) +VCC_CORE	(20) CPU_PWRGD
(2) S5_ON	(9) +5V_SUS	(14) CPU_COREPG	(21) ALINK_RST#
(3) +3V_S5, +1.2V_S5	(10) MAINON	(15) VLDT_RUN_ON	(22) PCI_RST#
(4) RSMRST	(11) +5V_RUN, +3.3V_RUN	(16) +1.2_VCCP	(23) LDT_RST#
(5) POWER_SW#	(12) VRON	(17) HWPG_1.2V	
(6) DNBSWON#	(13) +3.3V_ALW, +3.3V_SRC, +3.3V_RUN	(18) NB_PWRGD	
(7) SUSC#, SUSB#	(14) CPU_COREPG	(19) EC_PWRGD	



 QUANTA COMPUTER		
Title: SMBUS BLOCK		
Size: FX2	Document Number: FX2	Rev: 1A
Date: Friday, May 05, 2006	Sheet: 45 of 47	